CLC401 Fast Settling, Wideband High Gain Monolithic Op Amp

Check for Samples: CLC401

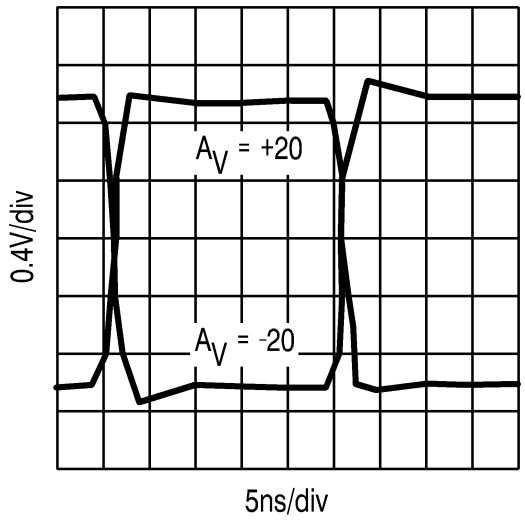
FEATURES

- **−3dB Bandwidth of 150MHz**
- **0.1% Settling in 10ns**
- **Low Power, 150mW**
- **Overload and Short Circuit Protected**
- **Stable Without Compensation**
- **Recommended Gain Range, ±7 to ±50**

APPLICATIONS

- **Flash, Precision A/D Conversion**
- **Photodiode, CCD Preamps**
- **IF Processors**
- **High Speed Modems, Radios**
- **Line Drivers**
- **DC Coupled Log Amplifiers**
- **High Speed Communications**

Pulse Response



DESCRIPTION

The CLC401 is a wideband, fast settling op amp designed for applications requiring gains greater than ±7. Constructed using an advanced complementary bipolar process and a proprietary design, the CLC401 features dynamic performance far beyond that of typical high speed monolithic op amps. For example, at a gain of +20, the −3dB bandwidth is 150MHz and the rise/fall time is only 2.5ns.

The wide bandwidth and linear phase (0.2° deviation from linear at 50MHz) and a very flat gain response makes the CLC401 ideal for many digital communication system applications. For example, demodulators need both DC coupling and high frequency amplification-requirements that are ordinarily difficult to meet.

The very fast 10ns settling to 0.1% and the ability to drive capacitive loads lend themselves well to flash A/D applications. Systems employing D/A converters also benefit from the settling time and also by the fact that current-to-voltage transimpedance amplification is easily accomplished.

The CLC401 provides a quick, effective design solution. Its stable operation over the entire ±7 to ±50 gain range precludes the need for external compensation. And, unlike many other high speed-op amps, the CLC401's power dissipation of 150mW is compatible with designs which must limit total power dissipation or power supply requirements.

The CLC401 is based on TI's proprietary op amp topology that uses current feedback instead of the usual voltage feedback. This unique design has many advantages over conventional designs (such as settling time that is relatively independent of gain), yet it is used in basically the same way (see the gain equations in Figure 17 and Figure 18). However, an understanding of the topology will aid in achieving the best performance. The discussion below will proceed for the non-inverting gain configuration with the inverting mode analysis being very similar.

Enhanced Solutions (Military/Aerospace)

SMD Number: 5962-89973

Space level versions also available.

CONNECTION DIAGRAM

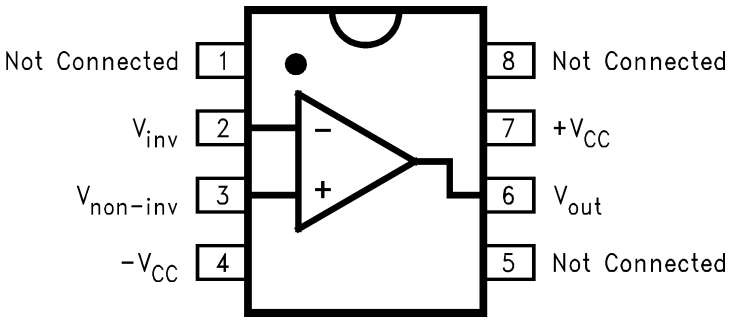


Figure 1. Pinout
PDIP & SOIC

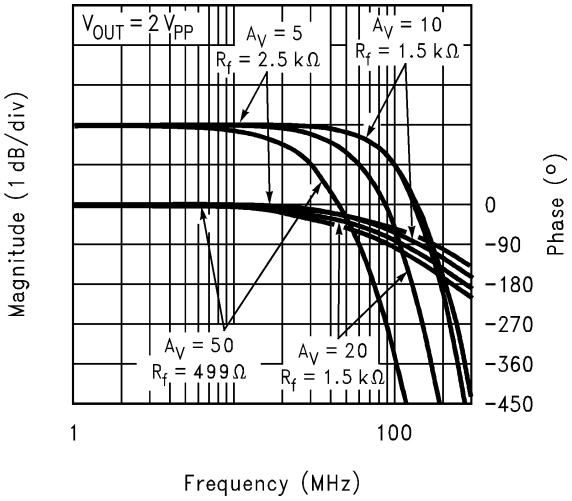


Figure 2. Non-Inverting Frequency Response

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)

Supply Voltage (V_{CC})		±7V
I_{OUT}	Output is short circuit protected to ground, but maximum reliability will be maintained if I_{OUT} does not exceed...	60mA
Common Mode Input Voltage		±V_{CC}
Differential Input Voltage		5V
Junction Temperature Range		+150°C
Operating Temperature Range		−40°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Solder Duration (+300°C)		10 sec

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The ELECTRICAL CHARACTERISTICS table specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

OPERATING RATINGS

Thermal Resistance		
Package	(θ_{JC})	(θ_{JA})
PDIP	70°C/W	125°C/W
SOIC	65°C/W	145°C/W

ELECTRICAL CHARACTERISTICS

(A_V= +20, V_{CC} = ±5V, R_L = 100Ω, R_f =1.5kΩ; unless specified).

Symbol	Parameter	Conditions	Typ	Max/Min Ratings (1)			Units
Ambient Temperature		CLC401AJ	+25°C	−40°C	+25°C	+85°C	
Frequency Domain Response							
SSBW	−3dB Bandwidth	V_{OUT} < $2V_{PP}$	150	>100	>100	>70	MHz
LSBW		V_{OUTt} < $5V_{PP}$	100	>65	>65	>55	MHz
	Gain Flatness	V_{OUT} < $2V_{PP}$					
GFPL	Peaking	<25MHz	0	<0.1	<0.1	<0.1	dB
GFPH	Peaking	>25MHz	0	<0.2	<0.2	<0.2	dB
GFR	Rolloff	<50MHz	0.2	<1.0	<1.0	<1.3	dB
LPD	Linear Phase Deviation	DC to 50MHz	0.2	<1.0	<1.0	<1.5	deg
Time Domain Response							
TRS	Rise and Fall Time	2V Step	2.5	<3.5	<3.5	<5.0	ns
TRL		5V Step	5	<7.0	<7.0	<8.0	ns
TS	Settling Time to ±0.1%	2V Step	10	<15	<15	<15	ns
OS	Overshoot	2V Step	0	<10	<10	<10	%
SR	Slew Rate		1200	>800	>800	>700	V/µs
Distortion And Noise Response							
HD2	2nd Harmonic Distortion	$2V_{PP}$, 20MHz	−45	<−35	<−35	<−35	dBc
HD3	3rd Harmonic Distortion	$2V_{PP}$, 20MHz	−60	<−50	<−50	<−45	dBc
	Equivalent Input Noise						
SNF	Noise Floor	>1MHz	−158	<−155	<−155	<−154	dBm (1Hz)
INV	Integrated Noise	1MHz to 150MHz	35	<50	<50	<55	µV

(1) Max/min ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

ELECTRICAL CHARACTERISTICS (continued)

(A_V= +20, V_{CC} = ±5V, R_L = 100Ω, R_f =1.5kΩ; unless specified).

Symbol	Parameter	Conditions	Typ	Max/Min Ratings (1)			Units
Static, DC Performance							
VIO	Input Offset Voltage (2)		3	±10.0	±6.0	±11.0	mV
DVIO	Average Temperature Coefficient		20	±50	–	±50	µV/°C
IBN	Input Bias Current (2)	Non-Inverting	10	±36	±20	±20	µA
DIBN	Average Temperature Coefficient		100	±200	–	±100	nA/°C
IBI	Input Bias Current (2)	Inverting	10	46	30	40	µA
DIBI	Average Temperature Coefficient		100	±200	–	±100	nA/°C
PSRR	Power Supply Rejection Ratio		55	50	50	50	dB
CMRR	Common Mode Rejection Ratio		55	50	50	50	dB
ICC	Supply Current (2)	No Load	15	21	21	21	mA
Miscellaneous Performance							
RIN	Non-Inverting Input	Resistance	200	>50	>100	>100	kΩ
CIN		Capacitance	0.5	<2.5	<2.5	<2.5	pF
RO	Output Impedance	at DC	0.2	<0.3	<0.3	<0.3	Ω
VO	Output Voltage Range	No Load	3.5	>3.0	>3.2	>3.2	V
CMIR	Common Mode Input Range	For Rated Performance	2.8	>2.0	>2.5	>2.5	V
IO	Output Current		60	>35	>50	>50	mA

(2) AJ-level: spec. is 100% tested at +25°C.

TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°, A_V = +20, V_{CC} = ±5V, R_L = 100Ω: Unless Specified).

Non-Inverting Frequency Response

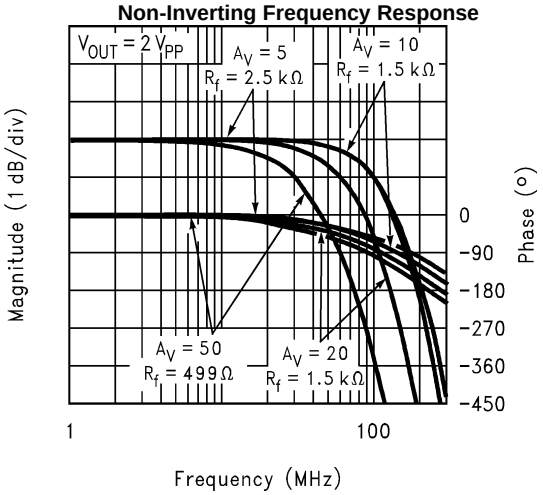


Figure 3.

Inverting Frequency Response

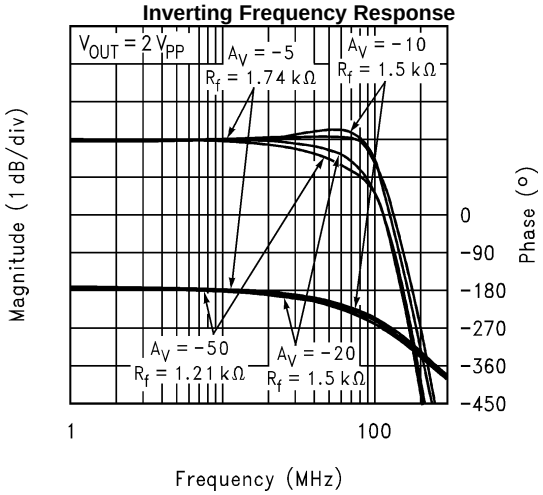


Figure 4.

Frequency Response for Various R_Ls

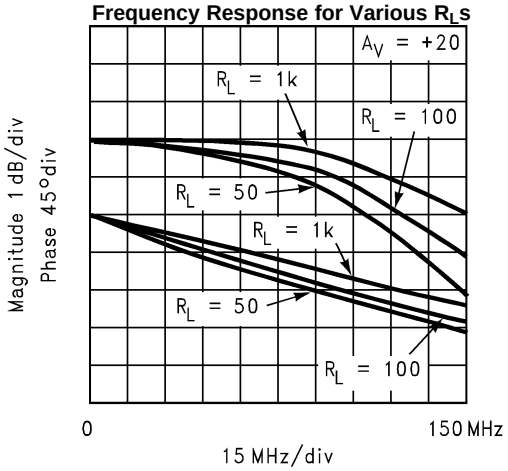


Figure 5.

Open-Loop Transimpedance Gain, Z(s)

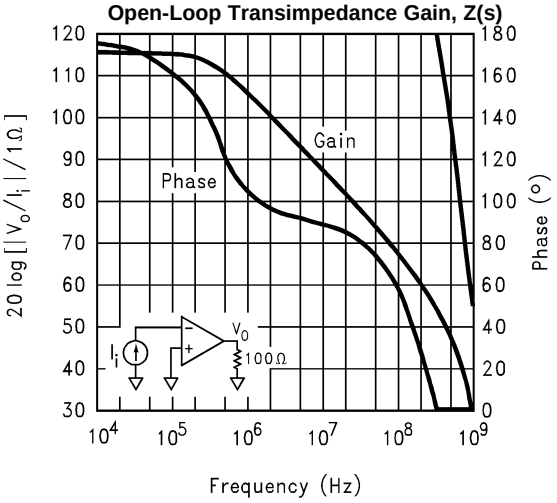


Figure 6.

2nd and 3rd Harmonic Distortion

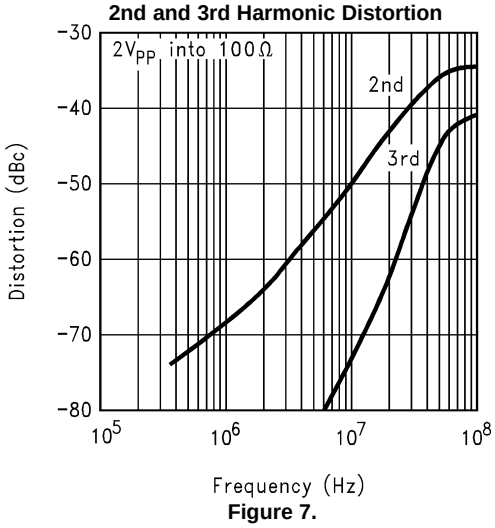


Figure 7.

2-Tone,3rd Order, Intermodulation Intercept

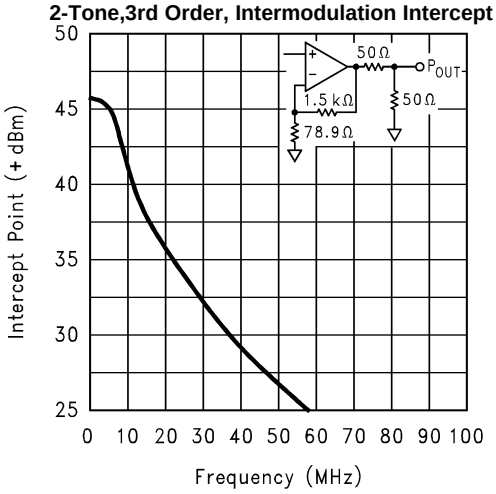


Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(T_A = 25°, A_V = +20, V_{CC} = ±5V, R_L = 100Ω: Unless Specified).

Equivalent Input Noise

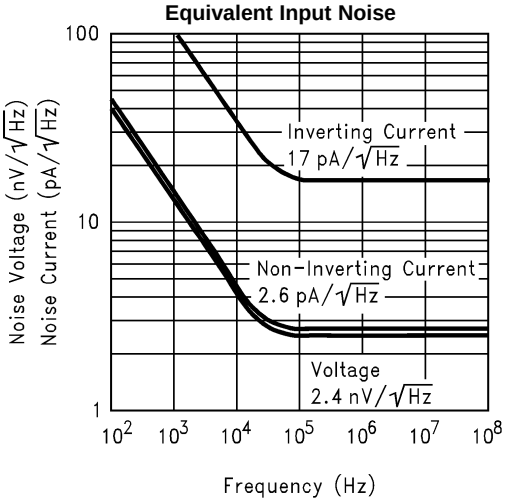


Figure 9.

CMRR and PSRR

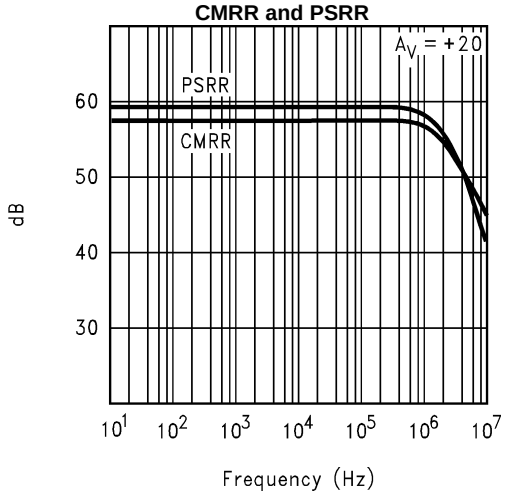


Figure 10.

Pulse Response

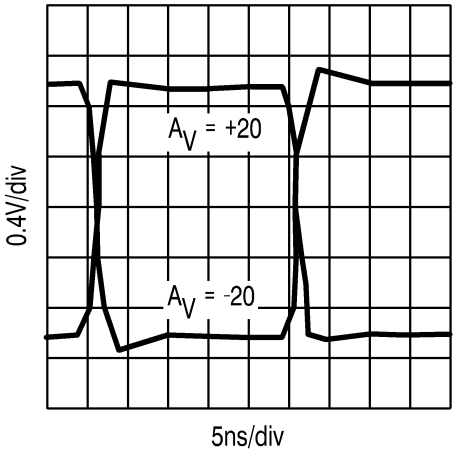


Figure 11.

Settling Time

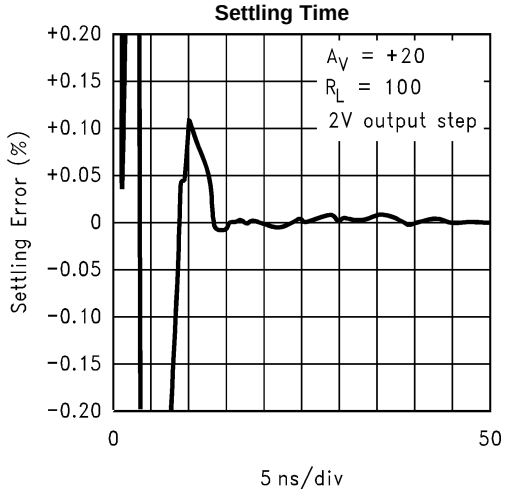


Figure 12.

Long-Term Settling Time

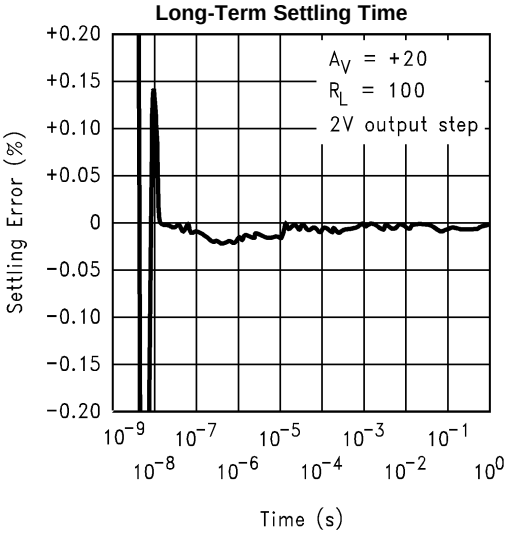


Figure 13.

Settling Time vs. Load Capacitance

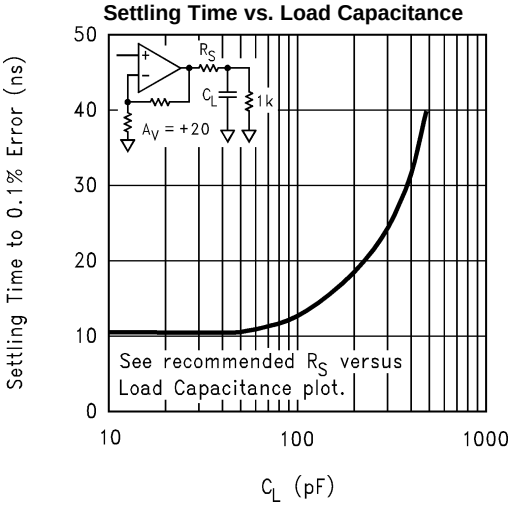


Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(T_A = 25°, A_V = +20, V_{CC} = ±5V, R_L = 100Ω: Unless Specified).

Recommended R_S vs. Load Capacitance

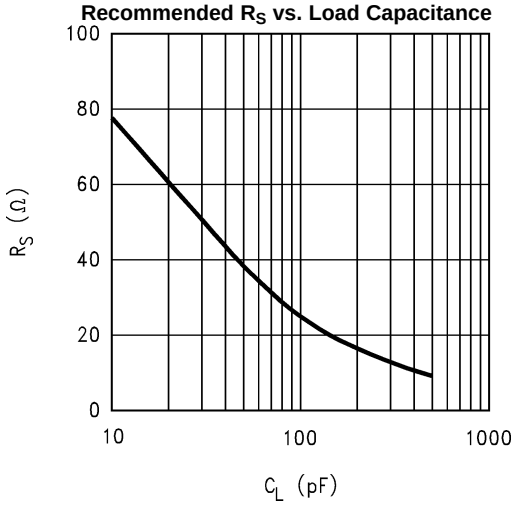


Figure 15.

Frequency Response, A_V = −1, R_f = 2.25kΩ

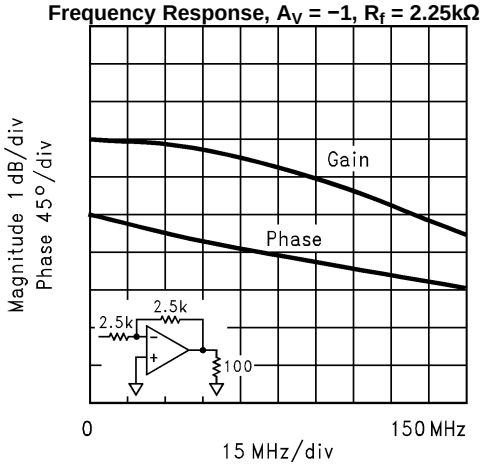


Figure 16.

Low Gain & Transimpedance Applications

The CLC401 may be used at gains down to unity (A_V = ±1) by choosing R_f according to Equation (4) in this datasheet. The curves to the right show performance at inverting unity gain with R_f = 2500Ω, a configuration appropriate for D/A converter buffering and other transimpedance applications.

APPLICATION DIVISION

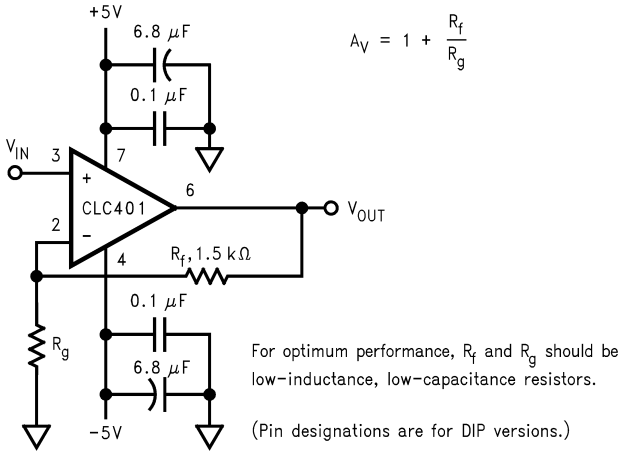


Figure 17. Recommended Non-Inverting Gain Circuit

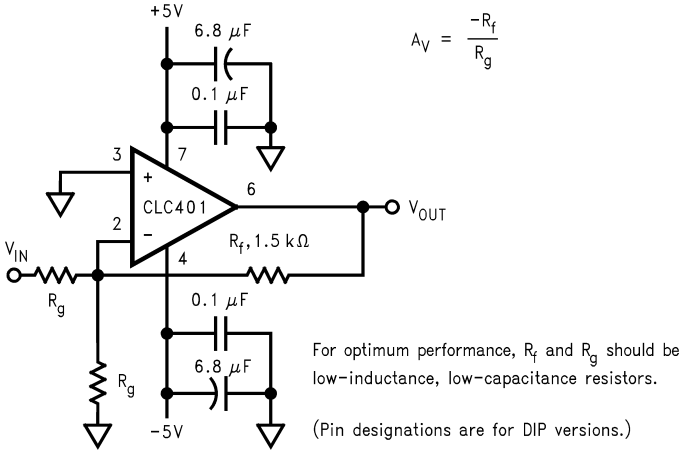


Figure 18. Recommended Inverting Gain Circuit

Understanding the Loop Gain

Referring to the equivalent circuit of Figure 19, any current flowing in the inverting input is amplified to a voltage at the output through the transimpedance gain shown on the plots (see Figure 6). This Z(s) is analogous to the open-loop gain of a voltage feedback amplifier.

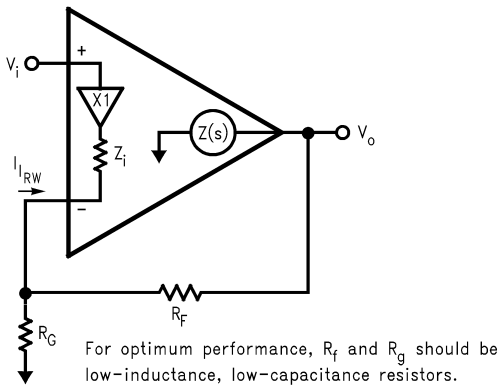


Figure 19. Current Feedback Topology

Developing the non-inverting frequency response for the topology of Figure 19 yields:

$$\frac{V_O}{V_i} = \frac{1 + R_f / R_g}{1 - 1 / LG} \quad (1)$$

where LG is the loop gain defined by,

$$LG = \frac{Z(s)}{R_f} \times \frac{1}{1 + Z_i / (R_f \,\|\, R_g)} \quad (2)$$

Equation 1 has a form identical to that for a voltage feedback amplifier with the differences occurring in the LG expression. For an idealized treatment, set $Z_i = 0$ which results in a very simple $LG = Z(s)/R_f$ (Derivation of the transfer function for the case where $Z_i = 0$ is given in Application Note AN300-1). Using the Z(s) (open-loop transimpedance gain) plot shown on the previous page and dividing by the recommended $R_f = 1.5k\Omega$, yields a large loop gain at DC. As a result, Equation 1 shows that the closed-loop gain at DC is very close to $(1+R_f/R_g)$.

At higher frequencies, the roll-off of Z(s) determines the closed-loop frequency response which, ideally, is dependent only on R_f. **The specifications reported on the previous pages are therefore valid only for the specified R = 1.5kΩ.** Increasing R from 1.5kΩ will decrease the loop gain and band width, while decreasing it will increase the loop gain possibly leading to inadequate phase margin and closed-loop peaking. Conversely, fixing R_f will hold the frequency response constant while the closed-loop gain can be adjusted using R_g.

The CLC401 departs from this idealized analysis to the extent that the inverting input impedance is finite. With the low quiescent power of the CLC401, Z ≅ 50Ω leading to drop in loop gain and bandwidth at high gain settlings, as given by Equation 2. The second term is Equation 2 accounts for the division in feedback current that occurs between Z_i and $R_f \| R_g$ at the inverting node of the CLC400. This decrease in bandwidth can be circumvented as described in “Increasing Bandwidth at High Gains.”

DC Accuracy and Noise

Since the two inputs for the CLC401 are quite dissimilar, the noise and offset error performance differs somewhat from that of a standard differential input amplifier. Specifically, the inverting input current noise is much larger than the non-inverting current noise. Also the two input bias currents are physically unrelated rendering bias current cancellation through matching of the inverting and non-inverting pin resistors ineffective.

In Equation 3, the output offset is the algebraic sum of the equivalent input voltage and current sources that influence DC operation. Output noise is determined similarly except that a root-sum-of-squares replaces the algebraic sum. R_S is the non-inverting pin resistance.

$$\text{Output Offset } V_O = \pm IBN \times R_S (1 + R_f/R_g) \pm VIO (1 + R_f/R_g) \pm IBI \times R_f \quad (3)$$

An important observation is that for fixed R_f, offsets as referred to the input improve as the gain is increased (divide all terms by $1+R_f/R_g$). A similar result is obtained for noise where noise figure improves as gain increases.

Selecting Between the CLC400 or CLC401

The CLC400 is intended for gains of ±1 to ±8 while the CLC401 is designed for gains of ±7 to ±50. Optimum performance is achieved with a feedback resistor of 250Ω with the CLC400 and 1.5Ω with the CLC401- this distinction may be important in transimpedance applications such as D/A buffering. Although the CLC400 can be used at higher gains, the CLC401 will provide a wider bandwidth because loop gain losses due to finite Z_i are lower with the larger CLC401 feedback resistor as explained above. On the other hand, the lower recommended feedback resistance of the CLC400 minimizes the output errors due to inverting input noise and bias currents.

Increasing Bandwidth At High Gains

Bandwidth may be increased at high closed-loop gains by adjusting R_f and $R_g$to make up for the losses in loop gain that occur at these high gain settlings due to current division at the inverting input. An approximate relationship my be obtained by holding the LG expression constant as the gain is changed from the design point used in the specifications (that is, R_f = 1.5kΩ and R_g = 79Ω). For the CLC401 this gives,

$$R_f = 2500 - 50A_V \text{ and } R_g = \frac{2500 - 50A_V}{A_V - 1} \quad (4)$$

where

- A_V is the desired non-inverting gain

Note that with A_V = +20 we get the specified R_f = 1.5kΩ, while at higher gains, a lower value gives stable performance with improved bandwidth.

Capacitive Feedback

Capacitive feedback should not be used with the CLC401 because of the potential for loop instability. See Application Note OA-7 for active filter realizations with the CLC401.

Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal coupling to the ground plane. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

Parasitic or load capacitance directly on the output will introduce additional phase shift in the loop degrading the loop phase margin and leading to frequency response peaking. A small series resistor before the capacitance effectively decouples this effect. The graphs on the preceding page illustrate the required resistor value and resulting performance vs. capacitance.

Precision buffed resistors (PRP8351 series from Precision Resistive Products) with low parasitic reactances were used to develop the data sheet specifications. Precision carbon composition resistors will also yield excellent results. Standard spirally-trimmed RN55D metal film resistors will work with the slight decrease in bandwidth due to their reactive nature at high frequencies.

Evaluation PC boards (part no. CLC730013 for through-hole and CLC730027 for SOIC) for the CLC401 are available.

REVISION HISTORY

Changes from Revision E (April 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	10

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