



GENERAL DESCRIPTION

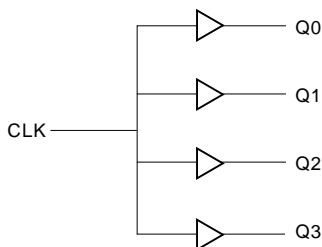


The ICS8304I is a low skew, 1-to-4 Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8304I is characterized at full 3.3V for input V_{DD} , and mixed 3.3V and 2.5V for output operating supply modes (V_{DDO}). Guaranteed output and part-to-part skew characteristics make the ICS8304I ideal for those clock distribution applications demanding well defined performance and repeatability.

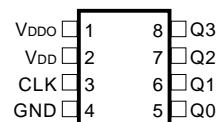
FEATURES

- 4 LVCMOS / LVTTTL outputs
- LVCMOS clock input
- CLK can accept the following input levels: LVCMOS, LVTTTL
- Maximum output frequency: 166MHz
- Output skew: 60ps (maximum)
- Part-to-part skew: 650ps (maximum)
- Small 8 lead SOIC package saves board space
- 3.3V input, outputs may be either 3.3V or 2.5V supply modes
- -40°C to 85°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS8304I

8-Lead SOIC

3.8mm x 4.8mm, x 1.47mm package body

M Package

Top View



TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V _{DDO}	Power		Output supply pin. Connect to 3.3V or 2.5V.
2	V _{DD}	Power		Positive supply pin. Connect to 3.3V.
3	CLK	Input	Pulldown	LVCMOS / LVTTTL clock input.
4	GND	Power		Power supply ground. Connect to ground.
5	Q0	Output		Single clock output. LVCMOS / LVTTTL interface levels.
6	Q1	Output		Single clock output. LVCMOS / LVTTTL interface levels.
7	Q2	Output		Single clock output. LVCMOS / LVTTTL interface levels.
8	Q3	Output		Single clock output. LVCMOS / LVTTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance				4	pF
C _{PD}	Power Dissipation Capacitance (per output)	V _{DD} , V _{DDO} = 3.465V			15	pF
R _{PULLUP}	Input Pullup Resistor			51		KΩ
R _{PULLDOWN}	Input Pulldown Resistor			51		KΩ
R _{OUT}	Output Impedance			7		Ω



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DDx}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, V_O	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, θ_{JA}	112.7°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Power Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				18	mA
I_{DDO}	Output Supply Current				11	mA

TABLE 3B. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		1.3	V
I_{IH}	Input High Current	$V_{DD} = V_{IN} = 3.465V$			150	μA
I_{IL}	Input Low Current	$V_{DD} = 3.465V, V_{IN} = 0V$	-5			μA
V_{OH}	Output High Voltage	Refer to NOTE 1	2.6			V
		$I_{OH} = -16mA$	2.9			V
		$I_{OH} = -100\mu A$	3			V
V_{OL}	Output Low Voltage	Refer to NOTE 1			0.5	V
		$I_{OL} = 16mA$			0.25	V
		$I_{OL} = 100\mu A$			0.15	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Section, "3.3V Output Load Test Circuit".



TABLE 4A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				166	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1	$f \leq 166MHz$	2		3.3	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 4	$f = 133MHz$			50	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4				600	ps
t_R	Output Rise Time	30% to 70%	250		500	ps
t_F	Output Fall Time	30% to 70%	250		500	ps
odc	Output Duty Cycle		40		60	%

All parameters measured at 166MHz unless noted otherwise.

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 3C. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				18	mA
I_{DDO}	Output Supply Current				11	mA

TABLE 3D. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		1.3	V
I_{IH}	Input High Current	$V_{DD} = V_{IN} = 3.465V$			150	μA
I_{IL}	Input Low Current	$V_{DD} = 3.465V, V_{IN} = 0V$	-5			μA
V_{OH}	Output High Voltage; NOTE 1		2.1			V
V_{OL}	Output Low Voltage; NOTE 1				0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Section, "3.3V/2.5V Output Load Test Circuit".



TABLE 4B. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				166	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1	$f \leq 166MHz$	2.3		3.7	ns
$tsk(o)$	Output Skew; NOTE 2, 4	$f = 133MHz$			60	ps
$tsk(pp)$	Part-to-Part Skew; NOTE 3, 4				650	ps
t_R	Output Rise Time	30% to 70%	250		500	ps
t_F	Output Fall Time	30% to 70%	250		500	ps
odc	Output Duty Cycle		40		60	%

All parameters measured at 166MHz unless noted otherwise.

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

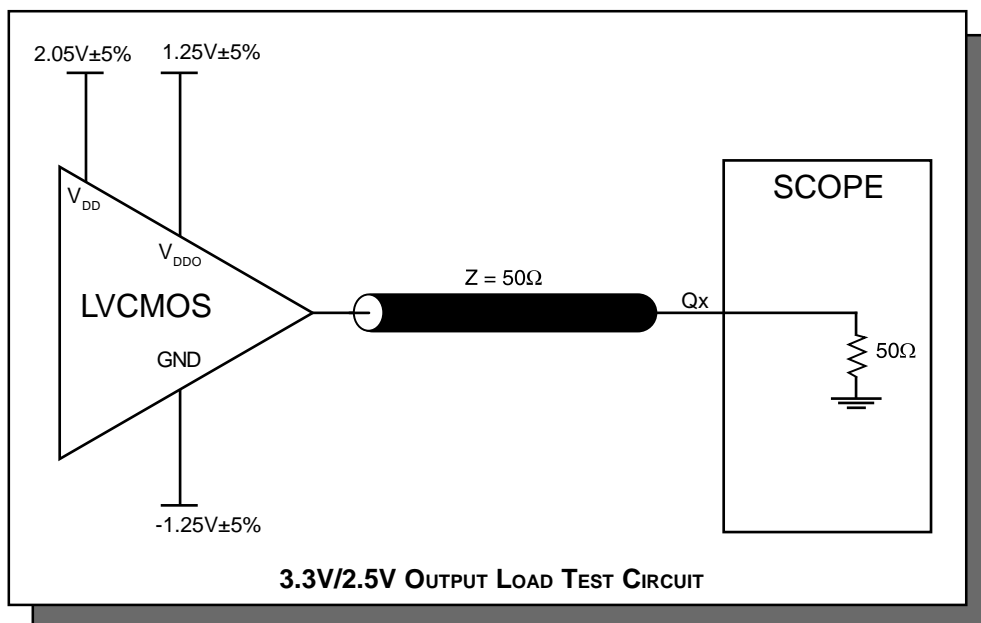
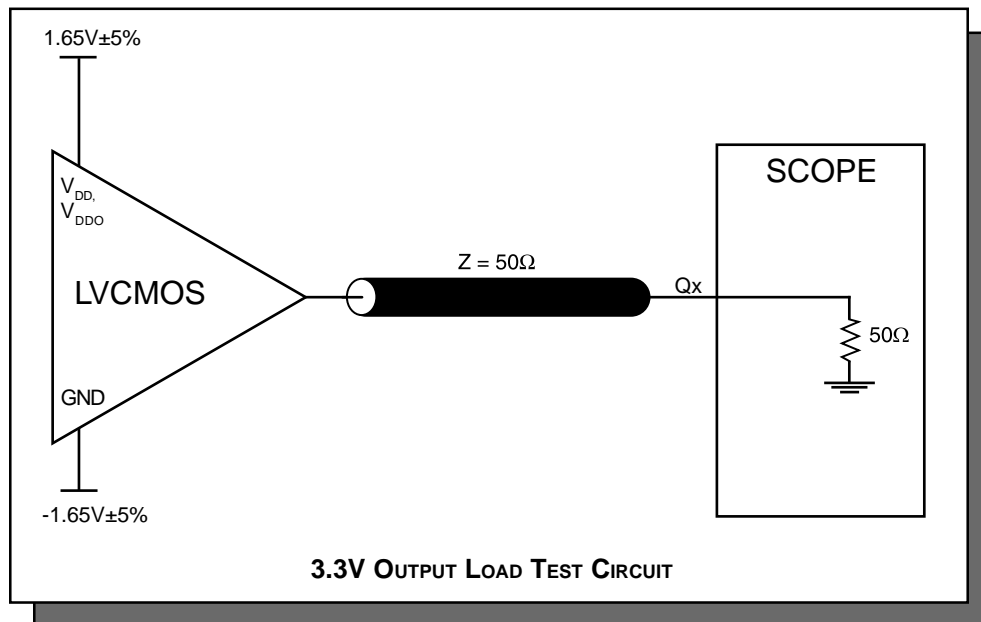
Measured at $V_{DDO}/2$.

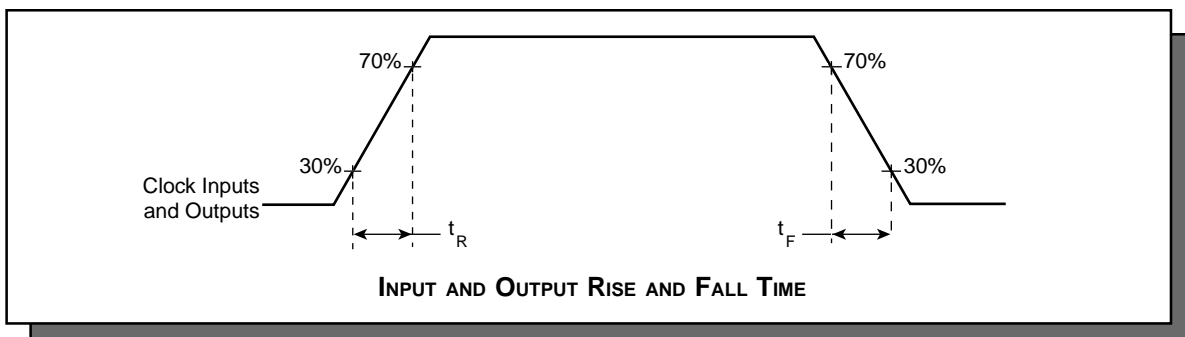
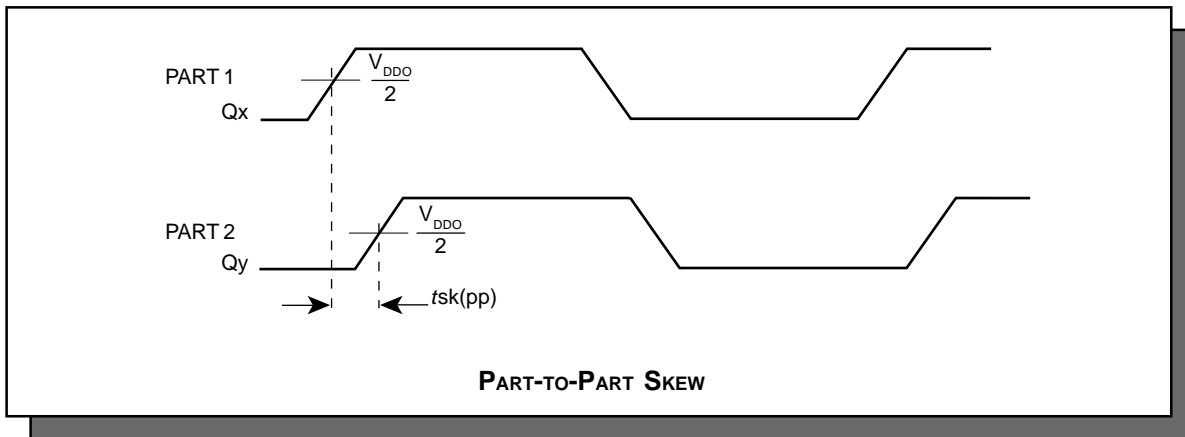
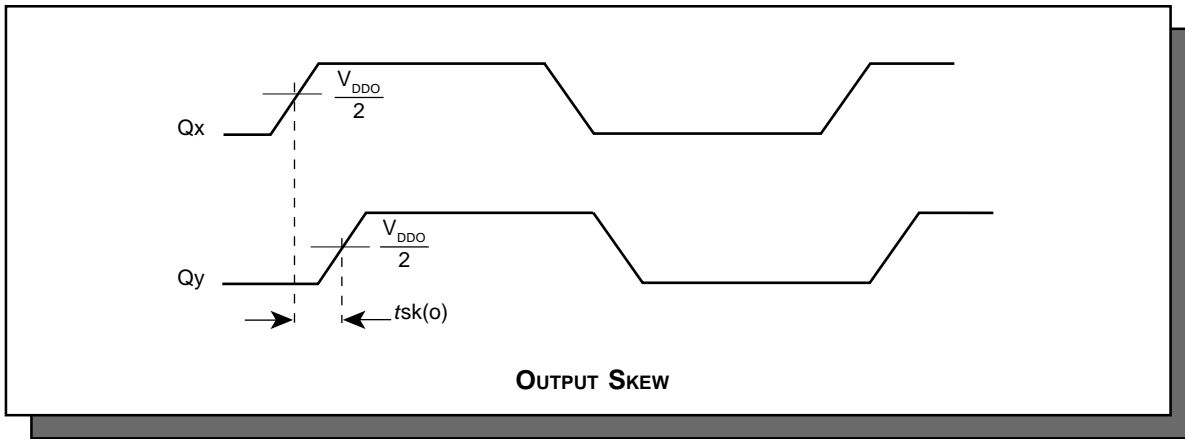
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



PARAMETER MEASUREMENT INFORMATION





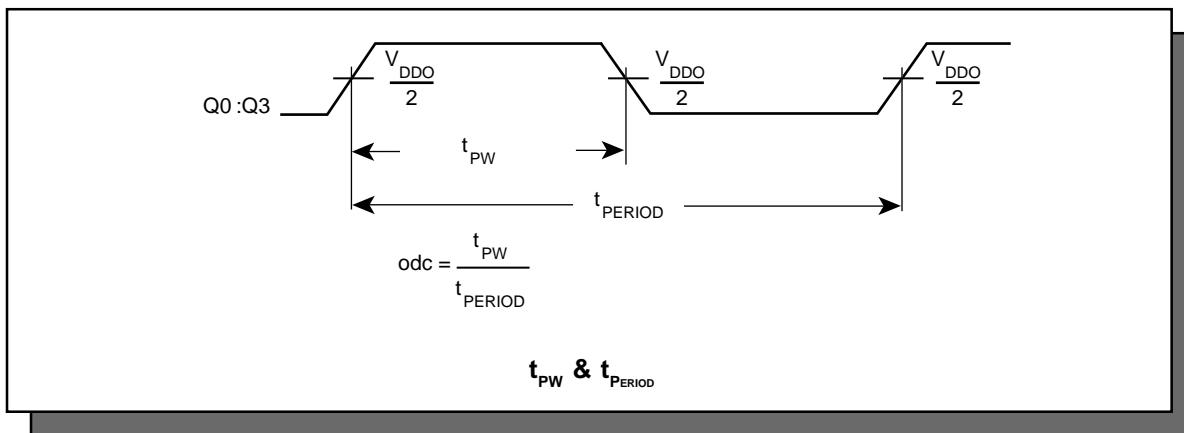
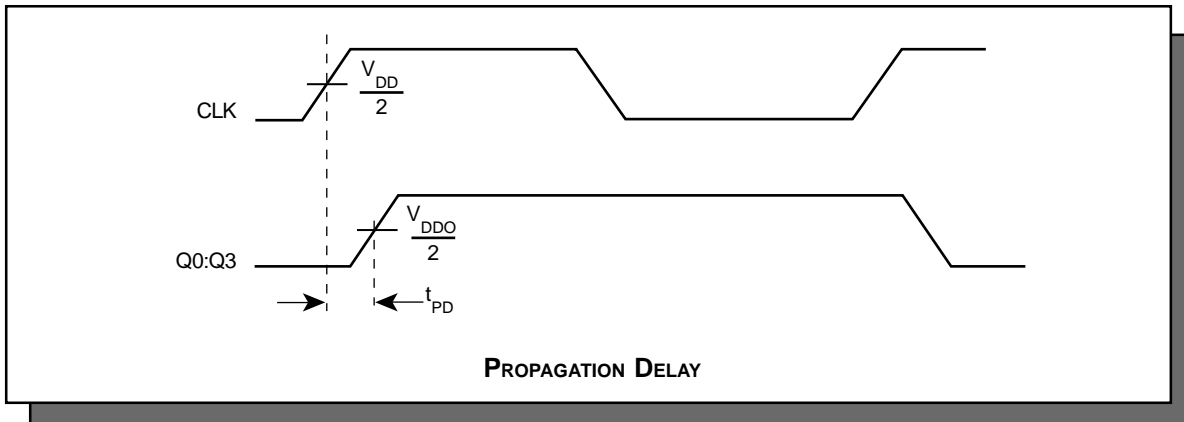




TABLE 5. θ_{JA} vs. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8304I is: 416



PACKAGE OUTLINE - SUFFIX M

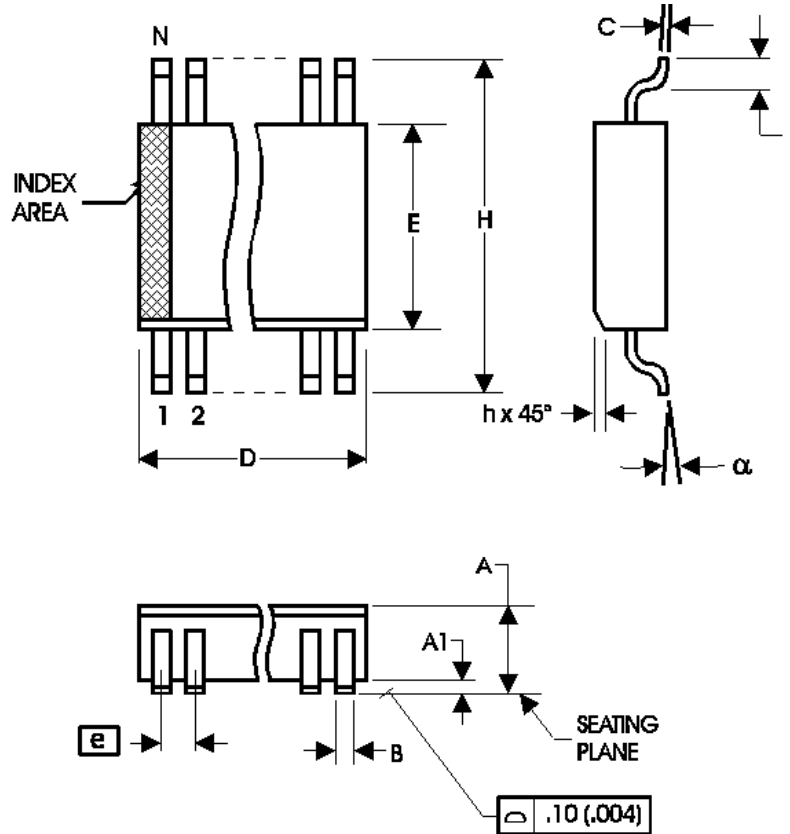


TABLE 6. PACKAGE DIMENSIONS - SUFFIX M

SYMBOL	Millimeters	
	MINIMUM	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012



Integrated
Circuit
Systems, Inc.

ICS8304I
LOW SKEW, 1-TO-4
LVCMOS / LVTTTL FANOUT BUFFER

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8304AMI	8304AMI	8 lead SOIC	96 per tube	-40°C to 85°C
ICS8304AMIT	8304AMI	8 lead SOIC on Tape and Reel	2500	-40°C to 85°C

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ICS8304I
LOW SKEW, 1-TO-4
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REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
B	3B	3	LVCMOS/LVTTTL DC Characteristics Table, added I_{OH} and I_{OL} Test Conditions to V_{OH} and V_{OL} rows.	4/4/02