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AN-9084

Smart Power Module, Motion SPM® 45 V3 Series User's Guide

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1. Introduction

This application note supports the Motion SPM® 45 V3 series. It should be used in conjunction with datasheets of Motion SPM® 45 V3 series, Fairchild's Motion SPM evaluation board user guides, and application notes which can be found on the web pages of which links are listed in *Section 8* Related Resources.

1.1 Design Concept

The key design objective of motion SPM product in the Motion SPM® 45 V3 series are to create minimized package and a low-power-consumption module with improved reliability. This is achieved by applying a new Insulated-Gate Bipolar Transistor (IGBT) of advanced silicon technology, optimized, gate drive ICs and improved ceramics substrate base transfer mold package.

Target applications are inverterized motor drives for low and medium power motor drives, such as washing machine, air conditioners and etc.

The third design advantage is the integrated NTC thermistor for temperature measuring of power chips (e.g. IGBTs, F'WDi's) on the same substrate. Most customers want to know the temperature of power chips precisely due to the impact on quality, reliability, and lifetime improvement. This desire is restricted because integrated power chips (e.g. IGBT, FWDi) inside modules are operated in high-voltage conditions. Therefore, instead of directly sensing the temperature of power chips, external NTC thermistor have been used for sensing the temperature of module or heat-sink. Although this method doesn't accurately reflect the temperature of power components; it is a simple and cost-effective method. However, the NTC thermistor of the Motion SPM® 45 V3 series are integrated with power chips on the same ceramic substrate to more accurately measure the temperature of power chips.

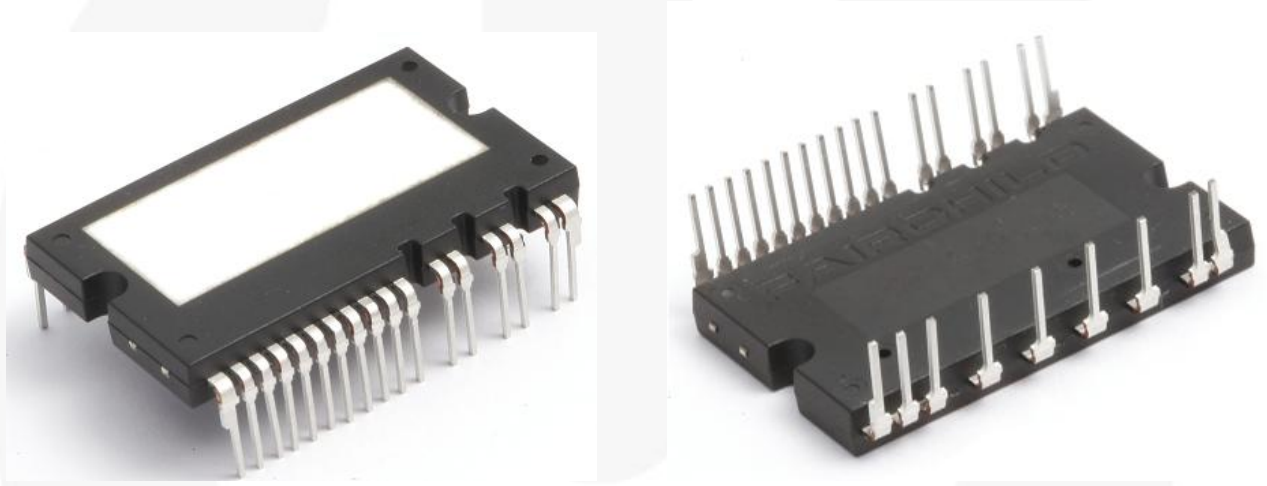


Figure 1. External View of Motion SPM® 45 V3 Series

Table 1. Product Line-up and Target Application

Fairchild Device	IGBT Rating	Motor Rating(1)	Target Application	Isolation Voltage
FNB41560Tx(2)	15 A / 600 V	0.75 kW / 220 V_{AC}	Washing Machine, Air Conditioner	V_{ISO} = 2000 V_{RMS} (Sine 60 Hz, 1-min between All Shorted Pins and Heat Sink)
FNB42060Tx(2)	20 A / 600 V	1.5 kW / 220 V_{AC}		
FNB43060Tx	30 A / 600 V	2.2 kW / 220 V_{AC}	Air Conditioner	

Notes:

1. These motor ratings are simulation results under following conditions: V_{AC} = 220 V, V_{DD} = 15 V, T_C = 100°C, T_J = 150°C, PF=0.8, MI=0.9, Motor efficiency=0.75, overload 150% for 1min.
2. In development.
   These motor ratings are general ratings, so may change by conditions.
3. An online loss and temperature simulation tool, Motion Control Design Tool (*https://www.fairchildsemi.com/design/design-tools/motion-control-design-tool/*), is recommended for choosing the right SPM product for the application.

1.2 Ordering Information

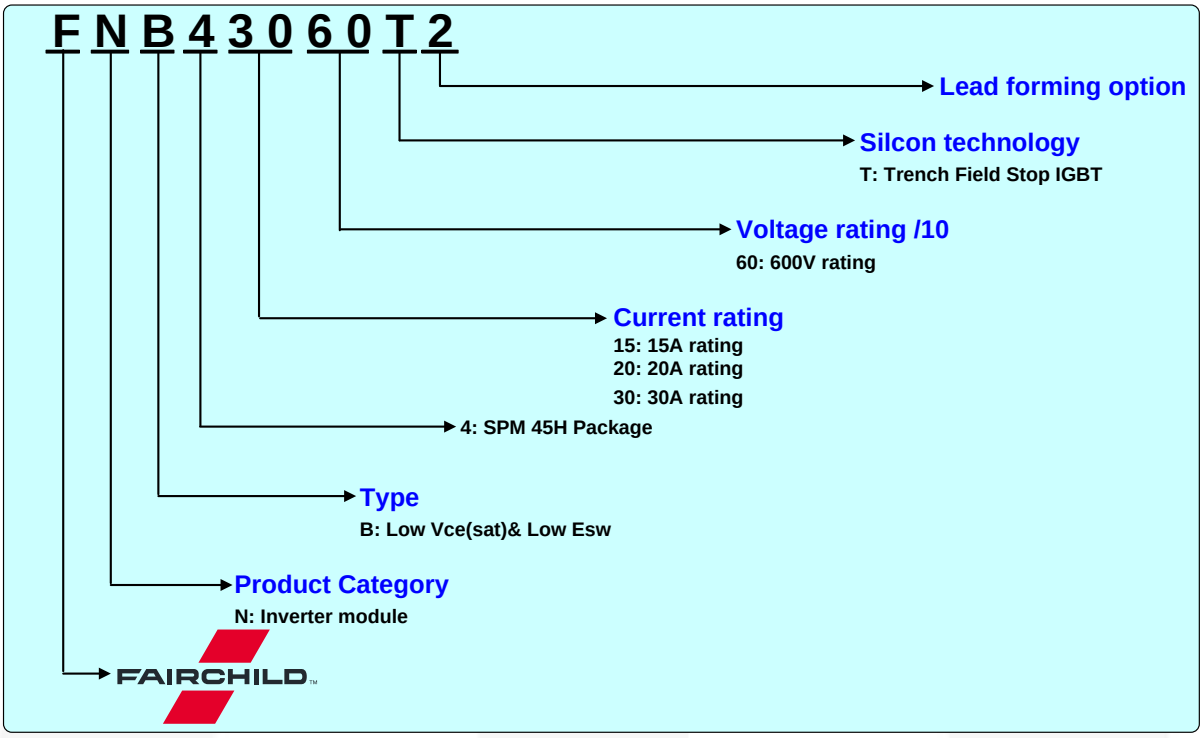


Figure 2. Ordering Information

1.3 Features and Integrated Functions

- Exceptionally small package size (WxD: 3 9mm x 23 mm) in three-phase inverter bridge module
- Advanced silicon technology IGBT and FWDi for low power loss and high ruggedness
- Built-in NTC thermistor for sensing temperature of power chips
- Easy PCB(print circuit board) layout due to built-in bootstrap diode and independent VS pin
- 600 V/15 A to 30 A ratings in one package (with identical mechanical layouts)
- High reliability due to advanced ceramic substrate transfer mold package
- Three-phase IGBT inverter bridge, including control ICs for gate drive and protection
  - High-Side: protection for control voltage without fault-out signal (V_{FO})
  - Low-Side: Under-Voltage Lockout (UVLO) and Over-Current Protection (OCP) through external shunt resistor with fault-out signal (V_{FO})
- Soft turn-off function during protection functions
- Single-grounded power supply and opto-coupler-less interface due to built-in HVIC
- Minimized standby current of drive IC (HVIC/LVIC) for energy regulation
- Active-High input signal logic resolves the startup and shutdown sequence restriction between V_{DD} (control supply voltage) and signal input, providing fail-safe operation with direct connection between the motion SPM product and a 3.3 V MCU or DSP without additional external sequence logic
- Isolation voltage rating of 2000 V_{rms} for one minute due to minimized package size

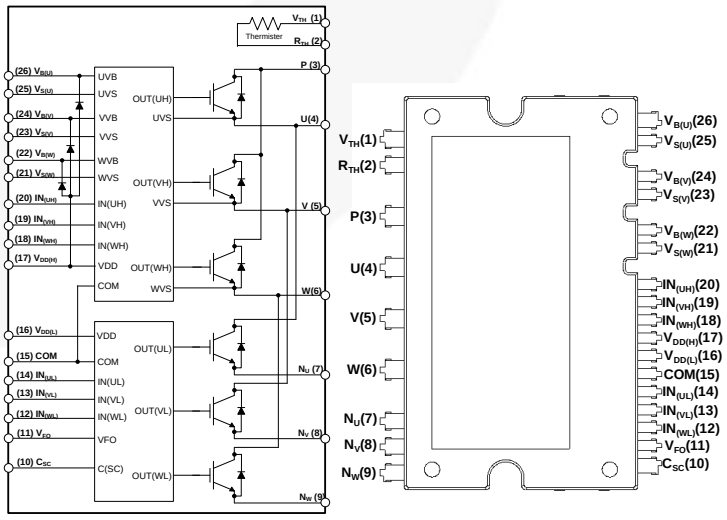


Figure 3. Internal Equivalent Circuit, Input / Output Pins and Package Top-View and Pin Assignment

2. Product Synopsis

This section discusses pin descriptions, electrical specifications, characteristics, and packaging.

Table 2. Pin Description

Pin Number	Name	Description
1	V_{TH}	Thermistor Bias Voltage
2	R_{TH}	Series Resistor for the Use of Thermistor (Temperature Detection)
3	P	Positive DC-Link Input
4	U	Output for U Phase
5	V	Output for V Phase
6	W	Output for W Phase
7	N_U	Negative DC-Link for U Phase
8	N_V	Negative DC-Link for V Phase
9	N_W	Negative DC-Link for W Phase
10	C_{SC}	Shutdown Input for Over-Current Protection
11	V_{FO}	Fault Output
12	$IN_{(WL)}$	Signal Input for Low-Side W Phase
13	$IN_{(VL)}$	Signal Input for Low-Side V Phase
14	$IN_{(UL)}$	Signal Input for Low-Side U Phase
15	COM	Common Supply Ground
16	$V_{DD(L)}$	Low-Side Common Bias Voltage for IC and IGBTs Driving
17	$V_{DD(H)}$	High-Side Common Bias Voltage for IC and IGBTs Driving
18	$IN_{(WH)}$	Signal Input for High-Side W Phase
19	$IN_{(VH)}$	Signal Input for High-Side V Phase
20	$IN_{(UH)}$	Signal Input for High-Side U Phase
21	$V_{S(W)}$	High-Side Bias Voltage Ground for W Phase IGBT Driving
22	$V_{B(W)}$	High-Side Bias Voltage for W Phase IGBT Driving
23	$V_{S(V)}$	High-Side Bias Voltage Ground for V Phase IGBT Driving
24	$V_{B(V)}$	High-Side Bias Voltage for V Phase IGBT Driving
25	$V_{S(U)}$	High-Side Bias Voltage Ground for U Phase IGBT Driving
26	$V_{B(U)}$	High-Side Bias Voltage for U Phase IGBT Driving

2.1 Detailed Pin Definition & Notification

- High-Side Bias Voltage Pins for Driving the IGBT/High-Side Bias Voltage Ground Pins for Driving the IGBTs
  - ► **Pins: $V_{B(U)}$-$V_{S(U)}$, $V_{B(V)}$-$V_{S(V)}$, $V_{B(W)}$-$V_{S(W)}$**
- These are drive power supply pins for providing gate drive power to the high-side IGBTs.
- The virtue of the ability to bootstrap the circuit scheme is that no external power supplies are required for the high-side IGBTs.
- Each bootstrap capacitor is charged from the V_{DD} supply during the on-state of the corresponding low side IGBT and low side diode.
- To prevent malfunctions caused by noise and ripple in supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted close to these pins.

- Low-Side Bias Voltage Pin / High-Side Bias Voltage Pins
  - ► **Pins: $V_{DD(L)}$, $V_{DD(H)}$**
- These are control supply pins for the built-in ICs.
- These two pins should be connected externally.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted close to these pins.

- Low-Side Common Supply Ground Pin
  - ► **Pin: COM**
- The motion SPM product common pin connects to the control ground for the internal ICs.
- Important! To avoid noise influences, the main power circuit current should not be allowed to blow through this pin. Signal Input Pins

- Signal input pins
  - ► **Pins: $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$, $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$**
- These pins control the operation of the built-in IGBTs.
- They are activated by voltage input signals. The terminals are internally connected to a Schmitt-trigger circuit composed of 5 V-class CMOS.
- The signal logic of these pins is active HIGH. The IGBT associated with each of these pins is turned ON when a sufficient logic voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the motion SPM product against noise influences.
- To prevent signal oscillations, an RC coupling is recommended as illustrated in 0.

- Short circuit and over current detection input pin
  - ► **Pin: C_{SC}**
- The current-sensing shunt resistor should be connected between the low-pass filter before the pin C_{SC} and the low-side ground COM to detect short-circuit or over current *(reference Figure 15).*
- The shunt resistor should be selected to meet the detection levels matched for the specific application.
  An RC filter should be connected to the C_{SC} pin to eliminate noise.
- The connection length between the shunt resistor and C_{SC} pin should be minimized.

- Fault Output Pin
  - ► **Pin: V_{FO}**
- This is the fault output alarm pin. An active low output is given on this pin for a fault state condition.
- The alarmed conditions are Over-Current Protection (OCP) or low-side bias Under-Voltage Lockout (UVLO) operation.
- The V_{FO} output is open-drain configured. The V_{FO} signal line should be pulled up to the 5 V logic power supply with approximately 4.7 kΩ resistance.

- Thermistor Bias Voltage
  - ► **Pin: V_{TH}**
- This is the bias voltage pin of the internal thermistor. It should be connected to the 3.3 or 5 V logic power supply.

- Series Resistor for the Use of Thermistor (Temperature Detection)
  - ► **Pin: R_{TH}**
- For case temperature (T_C) detection, this pin should be connected to an external series resistor.
- The external series resistor should be selected to meet the detection range matched for the specification of each application *(for details, refer to Figure 30).*

- Positive DC-Link Pin
  - ► **Pin: P**
- This is the DC-link positive power supply pin of the inverter.
- It is internally connected to the collectors of the high-side IGBTs.
- To suppress the surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin (typically, metal film capacitors are used).

- Negative DC-Link Pin
  - ► **Pins: N_U, N_V, N_W**
- These are the DC-link negative power supply pins (power ground) of the inverter.
- These pins are connected to the low-side IGBT emitters of the each phase.

- Inverter Power Output Pin
  - ► **Pins: U, V, W**
- Inverter output pins for connecting to the inverter load (e.g. motor).

2.2 Absolute Maximum Ratings

T_J = 25°C, unless otherwise specified.

Table 3. Inverter Part

Symbol	Parameter	Conditions		Rating	Unit
V_{PN}	Supply Voltage	Applied between P – N_U, N_V, N_W		450	V
$V_{PN(Surge)}$	Supply Voltage (Surge)	Applied between P – N_U, N_V, N_W		500	V
V_{CES}	Collector – Emitter Voltage			600	V
$\pm I_C$	Each IGBT Collector Current	T_C=25°C, T_J < 150°C	FNB41560Tx	(15)	A
			FNB42060Tx	(20)	
			FNB43060Tx	30	
$\pm I_{CP}$	Each IGBT Collector Current (Peak)	T_C=25°C, T_J < 150°C, Under 1 ms Pulse Width	FNB41560Tx	(30)	A
			FNB42060Tx	(40)	
			FNB43060Tx	60	
P_C	Collector Dissipation	T_C=25°C per One Chip	FNB41560Tx	TBD	W
			FNB42060Tx	TBD	
			FNB43060Tx	59	
T_J	Operating Junction Temperature[4]			-40~150	°C

Note:
4. The maximum junction temperature rating of the power chips integrated within the Motion SPM® 45 V3 series are 150°C.

Table 4. Control Part

Symbol	Parameter	Conditions	Rating	Unit
V_{DD}	Control Supply Voltage	Applied between $V_{DD(H)}$, $V_{DD(L)}$ - COM	20	V
V_{BS}	High-Side Control Bias Voltage	Applied between $V_{B(X)}$ – $V_{S(X)}$	20	V
V_{IN}	Input Signal Voltage	Applied between $IN_{(xH)}$, $IN_{(xL)}$ - COM	-0.3~V_{DD}+0.3	V
V_{FO}	Fault Supply Voltage	Applied between V_{FO} - COM	-0.3~V_{DD}+0.3	V
I_F	Fault Current	Sink Current at V_{FO} Pin	1	mA
V_{SC}	Current Sensing Input Voltage	Applied between C_{SC} - COM	-0.3~V_{DD}+0.3	V

Table 5. Bootstrap Diode Part

Symbol	Parameter	Conditions	Rating	Unit
V_{RRM}	Maximum Repetitive Reverse Voltage		600	V
I_F	Forward Current	T_C=25°C, T_J < 150°C	0.5	A
I_{FP}	Forward Current (Peak)	T_C=25°C, T_J < 150°C, Under 1 ms Pulse Width	2	A
T_J	Operating Junction Temperature		-40~150	°C

Table 6. Total System

Symbol	Parameter	Conditions	Rating	Unit
$V_{PN(PROT)}$	Self Protection Supply Voltage Limit (Short-Circuit Protection Capability)	V_{DD}, V_{BS}=13.5~16.5 V, T_J=150°C, Non-Repetitive, < 2 µs	400	V
T_{STG}	Storage Temperature		-40~125	°C
V_{ISO}	Isolation Voltage	60 Hz, Sinusoidal, 1-Minute, Connect Pins to Heat Sink Plate	2000	V_{rms}

Table 7. Thermal Resistance

Symbol	Parameter	Conditions		Rating	Unit
$R_{th(j-c)Q}$	Junction-to-Case Thermal Resistance	Inverter IGBT Part (per 1/6 Module)	FNB41560Tx	TBD	°C/W
			FNB42060Tx	TBD	
			FNB43060Tx	2.1	
$R_{th(j-c)F}$		Inverter FWDi Part (per 1/6 Module)	FNB41560Tx	TBD	
			FNB42060Tx	TBD	
			FNB43060Tx	2.8	

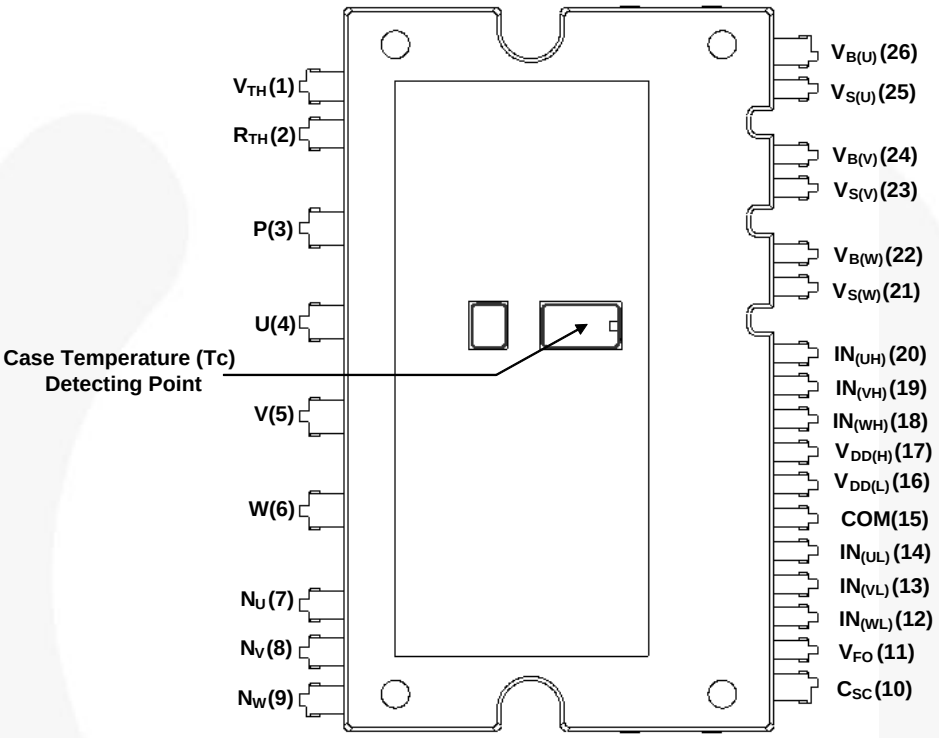


Figure 4. Case Temperature (T_C) Detecting Point

Table 8. Recommended Operating Conditions (Based on FNB43060Tx)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{PN}	Supply Voltage	Applied between P - N_U, N_V, N_W		300	400	V
V_{DD}	Control Supply Voltage	Applied between V_{DD} - COM	14.0	15.0	16.5	V
V_{BS}	High-Side Bias Voltage	Applied between $V_{B(X)} – V_{S(X)}$	13.0	15.0	18.5	V
dV_{DD}/dt, dV_{BS}/dt	Control Supply Variation		-1		+1	V/µs
t_{dead}	Blanking Time for Preventing Arm-Short	For Each Input Signal	1.0			µs
f_{PWM}	PWM Input Signal	- 40°C < T_J < 150°C			20	kHz
V_{SEN}	Voltage for Current Sensing	Applied between N_U, N_V, N_W - COM (Including Surge Voltage)	-4		4	V
$P_{WIN(ON)}$	Minimum Input Pulse Width[5]		1.2			µs
$P_{WIN(OFF)}$			1.2			

Note:

5. This product may not make response if the input pulse width is less than the recommended value.

2.3 Electrical Characteristics

T_J = 25°C, unless otherwise specified.

Table 9. Inverter Part (Based on FNB43060Tx)

Symbol		Parameter	Conditions		Min.	Typ.	Max.	Unit
$V_{CE(SAT)}$		Collector–Emitter Saturation Voltage	V_{DD}, V_{BS}=15 V, V_{IN}=5 V, I_C=30 A	T_J=25°C		1.65	2.25	V
V_F		FWDi Forward Voltage	V_{IN}=0 V, I_F=30 A	T_J=25°C		2.00	2.60	
HS	t_{ON}	Switching Times	V_{PN}=300 V, V_{DD} =15 V, V_{BS}=15 V, I_C=30 A T_J=25, V_{IN}=0 V ↔5 V, Inductive Load(6)		0.45	0.85	1.35	µs
	$t_{C(ON)}$					0.20	0.60	
	t_{OFF}					0.70	1.20	
	$t_{C(OFF)}$					0.15	0.45	
	t_{rr}					0.10		
LS	t_{ON}				0.5	0.90	1.40	
	$t_{C(ON)}$					0.30	0.60	
	t_{OFF}					0.80	1.30	
	$t_{C(OFF)}$					0.15	0.45	
	t_{rr}					0.15	-	
I_{CES}		Collector – Emitter Leakage Current	V_{CE}=V_{CES}				1	mA

Note:

6. t_{ON} and t_{OFF} include the propagation delay of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching times of the IGBT itself under the given gate driving condition internally. *For the detailed information, see Figure 5 and Figure 6.*

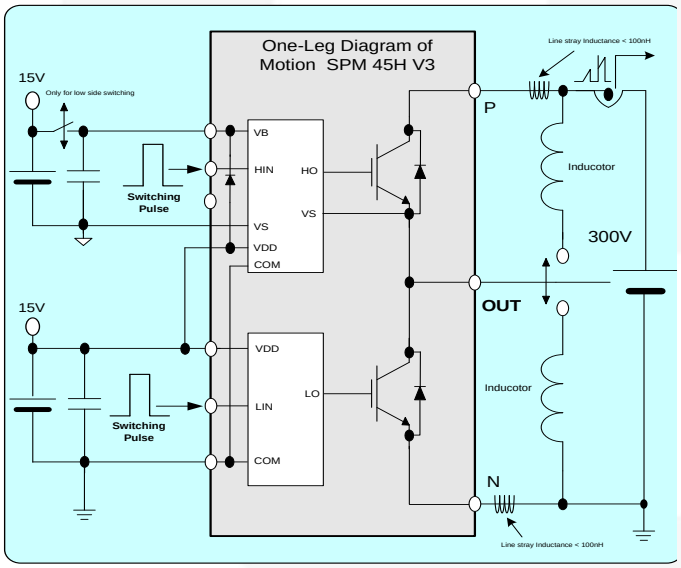


Figure 5. Switching Evaluation Circuit

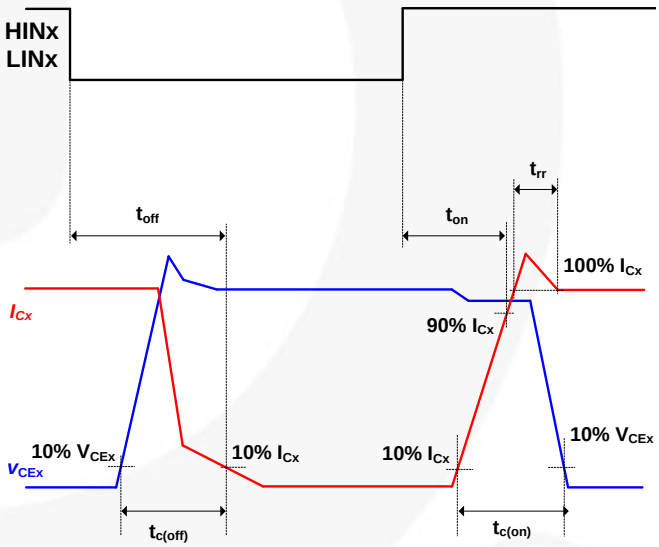


Figure 6. Switching Time Definition

Table 11. Control Part (Based on FNB43060Tx)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{QDDH}	Quiescent V_{DD} Supply Current	$V_{DD(H)}$ =15 V, IN(xH)=0 V	$V_{DD(H)}$ - COM			0.10	mA
I_{QDDL}		$V_{DD(L)}$ =15 V, IN(xL)=0 V	$V_{DD(L)}$ - COM			2.65	
I_{PDDH}	Operating V_{DD} Supply Current	$V_{DD(H)}$ =15 V, f_{PWM}=20 kHz, Duty=50%, Applied to One PWM Signal Input for High Side	$V_{DD(H)}$ - COM			0.15	mA
I_{PDDL}		$V_{DD(L)}$ =15 V, f_{PWM}=20 kHz, Duty=50%, Applied to One PWM Signal Input for High Side	$V_{DD(L)}$ - COM			4.0	mA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{BS}=15 V, IN(xH)=0 V	Applied between VB(x) –VS(x)			0.30	mA
I_{PBS}	Operating V_{BS} Supply Current	V_{DD}, V_{BS}=15 V, f_{PWM}=20 kHz, Duty=50%, Applied to One PWM Signal Input for High Side	Applied between VB(x) –VS(x)			2.00	mA
V_{FOH}	Fault Output Voltage	V_{DD}=15 V, V_{SC}=0 V, V_F Circuit: 4.7 kΩ to 5 V Pull-up		4.5			V
V_{FOL}		V_{DD}=15 V, V_{SC}=1 V, V_F Circuit: 4.7 kΩ to 5 V Pull-up				0.5	
$V_{SC(ref)}$	Over current (including short circuit) Trip Level	V_{DD}=15 V[7]	C_{SC} - COM	0.45	0.50	0.55	V
UV_{DDD}	Supply Circuit, Under-Voltage Protection	Detection Level		10.5		13.0	V
UV_{DDR}		Reset Level		11.0		13.5	
UV_{BSD}		Detection Level		10.0		12.5	
UV_{BSR}		Reset Level		10.5		13.0	
t_{FOD}	Fault-Out Pulse Width			30			µs
$V_{IN(ON)}$	ON Threshold Voltage	Applied between $IN_{(xH)}$, $IN_{(xL)}$ - COM				2.6	V
$V_{IN(OFF)}$	OFF Threshold Voltage			0.8			
R_{TH}	Resistance of Thermistor	@T_{TH} = 25°C[8]			47		kΩ
		@T_{TH}=100°C			2.9		

Note:

7. Short-circuit current protection function is for low sides only.
8. T_{TH} is the temperature of thermistor itself. To know case temperature (Tc), please make the experiment considering application of user.

2.4 Package

Since heat dissipation is an important factor that limits the power module's current capability, the heat dissipation characteristics are critical in determining the Motion SPM® 45 V3 series performance. A trade-off exists among heat dissipation characteristics, package size, and isolation characteristics. The key to a good package technology lies in the accomplishment of optimization package size while maintaining outstanding heat dissipation characteristics without compromising the isolation rating.

In the Motion SPM® 45 V3 series , technology was developed in which bare ceramic with good heat dissipation characteristic is attached directly to the lead frame. This technology already applied in SPM3, but was improved through new adhesion methods. This made it possible to achieve improved reliability and heat dissipation, while maintaining cost effectiveness. Figure 7 shows the package outline and the cross-sections of the Motion SPM® 45 V3 series package. And distances for an isolation are shown in Figure 8 and Figure 9.

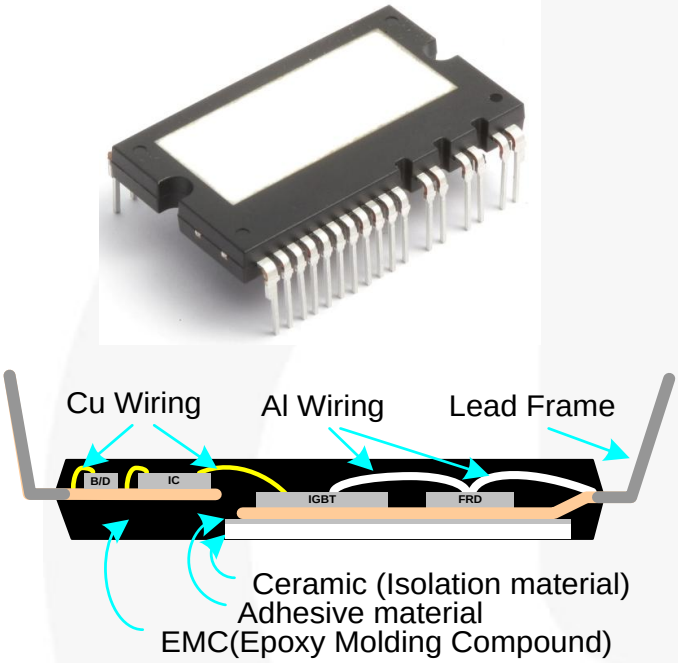


Figure 7. Vertical Structure of Motion SPM® 45 V3 Series

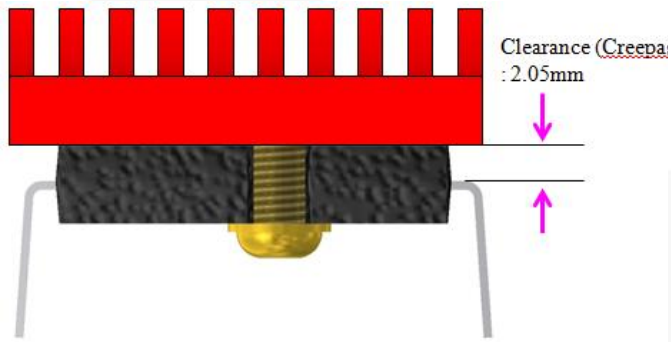


Figure 8. Distance for Isolation from pints to Heat Sink

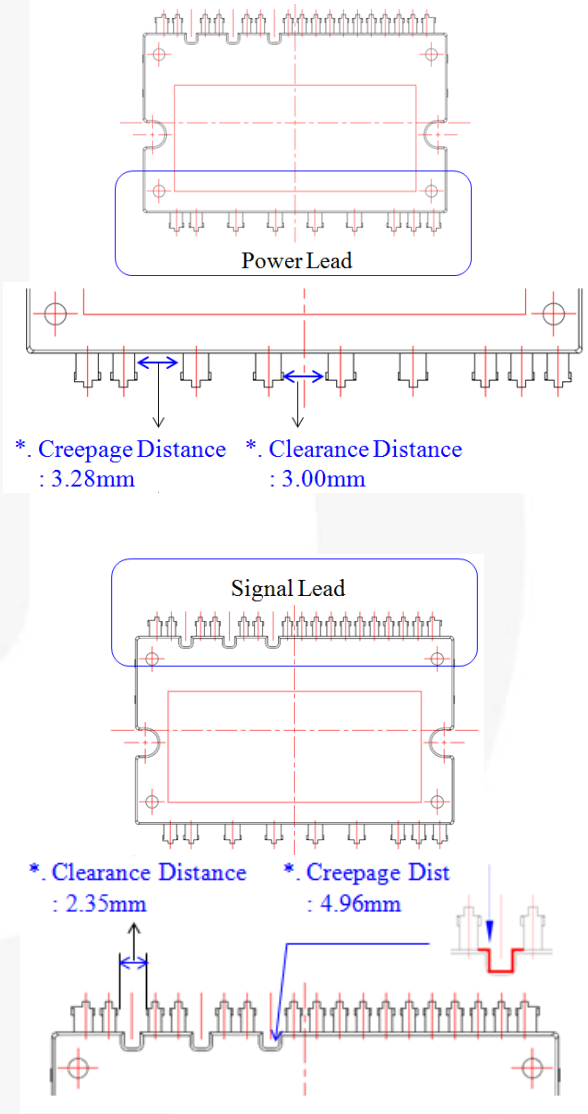


Figure 9. Distance for Isolation from Pin to Pin

3. Outline & Pin Description

Outline Drawings

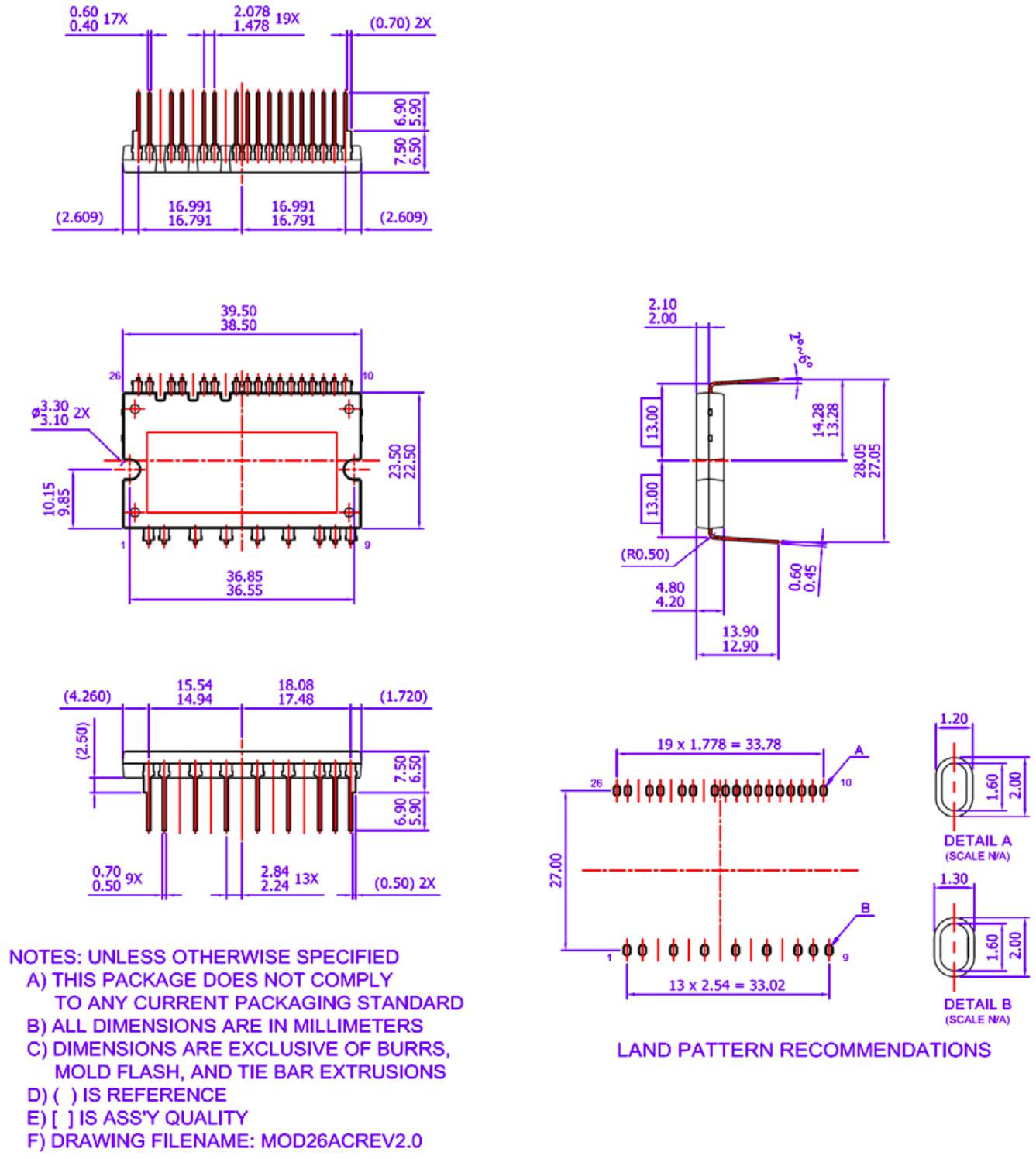


Figure 10. FNB4xx60T2

4. Operating Sequence for Protections

4.1 Over-Current Protection (OCP)

Motion SPM® 45 V3 series use an external shunt resistor for the over-current detection, as shown in Figure 11. The LVIC has built-in over current protection that senses the voltage to the C_{SC} pin and, if this voltage exceeds the $V_{SC(REF)}$ (the threshold voltage trip level of protection function) specified in the devices datasheets($V_{SC(REF)}$, Typ. is 0.5 V), a fault signal is asserted and the all three lower arm IGBTs are turned off. Short circuit is included to over current situation. Typically the maximum short-circuit current magnitude is gate voltage dependent. A higher gate voltage (V_{DD} & V_{BS}) is resulted in a larger short circuit current. To avoid this potential problem, the maximum short-circuit trip level is generally set to below 1.7 times the nominal rated collector current. The over-current protection-timing chart is shown in Figure 12.

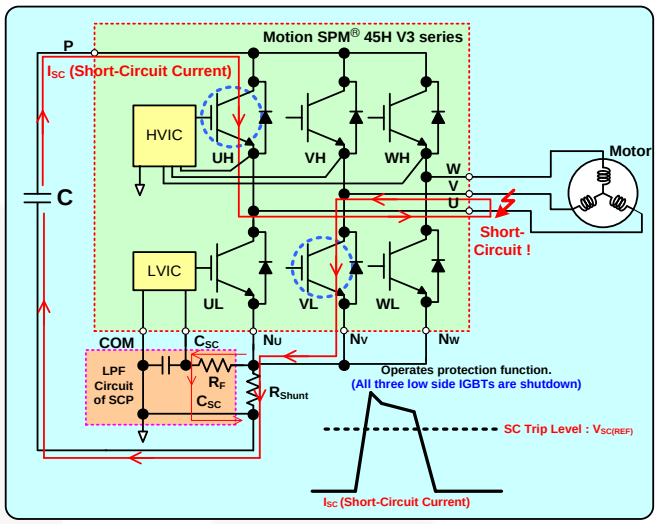


Figure 11. Operation of Short-Circuit Current Protection

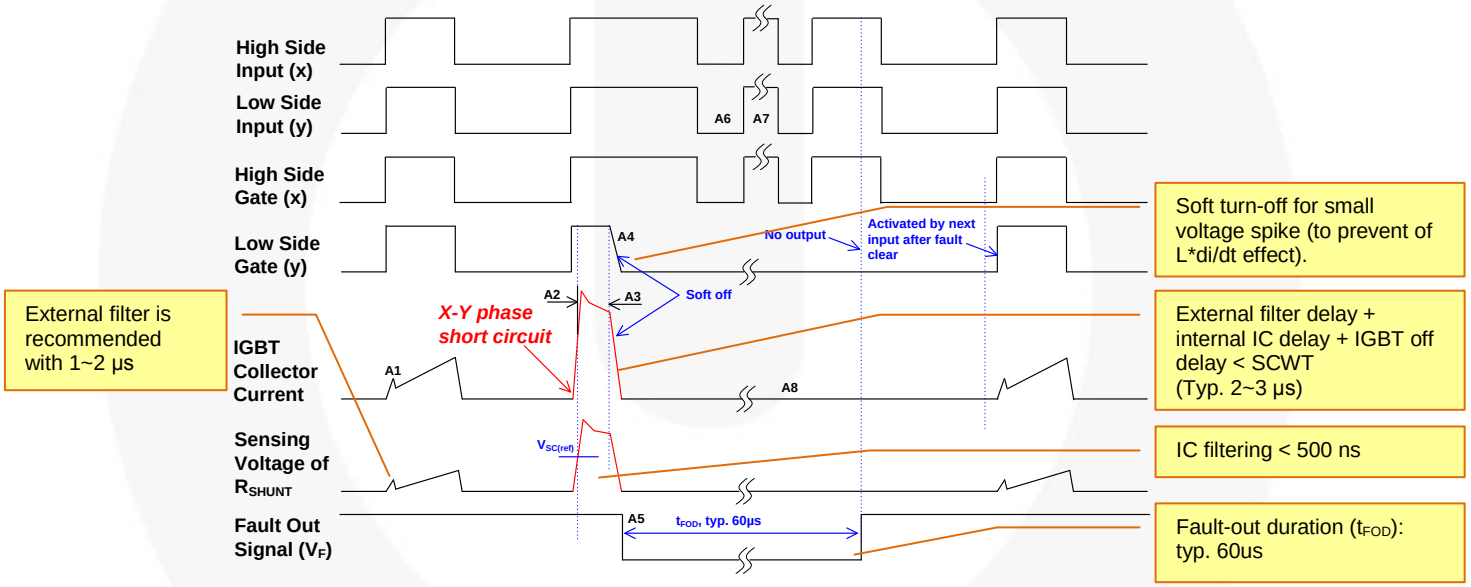


Figure 12. Timing Chart of Over-Current Protection Function

Notes:

9. A1-Normal operation: IGBTs on and carrying current.
10. A2-Over-current detection (OC trigger).
11. A3-Hard IGBTs gate interrupt.
12. A4-Low side IGBTs turn off by soft-off function.
13. A5-Fault output timer operation start with internal delay (Typ. 2.5 µs), t_{FOD}=Typ. 60 µs.
14. A6-Input "L": Low side IGBTs OFF state.
15. A7-Input "H": Low side IGBTs input ON state, but during the active period of fault output the IGBT doesn't turn ON.
16. A8-Low side IGBTs keeps OFF state.

4.3 Under-Voltage Lockout Protection

The low side gate drive IC has an under-voltage lockout protection (UVLO) function to protect the low-side IGBTs from operation with insufficient gate driving voltage. A timing chart for this protection is shown in Figure 13.

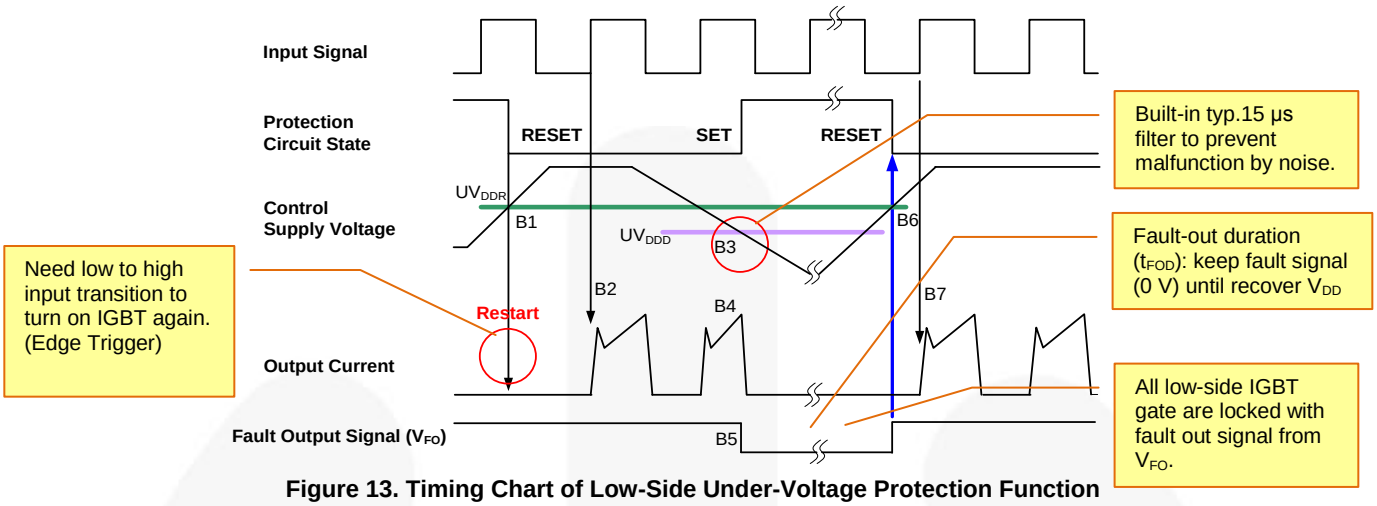


Figure 13. Timing Chart of Low-Side Under-Voltage Protection Function

Notes:

17. B1-control supply voltage rise: after the voltage rises UV_{DDR}, the circuits starts to operate when the next input is applied.
18. B2-normal operation: IGBT ON and carrying current.
19. B3-under-voltage detection (UV_{DDD}).
20. B4-IGBT OFF in spite of control input is alive.
21. B5-fault output signal starts.
22. B6-under-voltage reset (UV_{DDR}).
23. B7-normal operation: IGBT ON and carrying current.

The high side gate drive IC has an under-voltage lockout function to protect the high-side IGBT from insufficient gate driving voltage. A timing chart for this protection is shown in Figure 14. A fault-out alarm is not given for low at high side bias conditions.

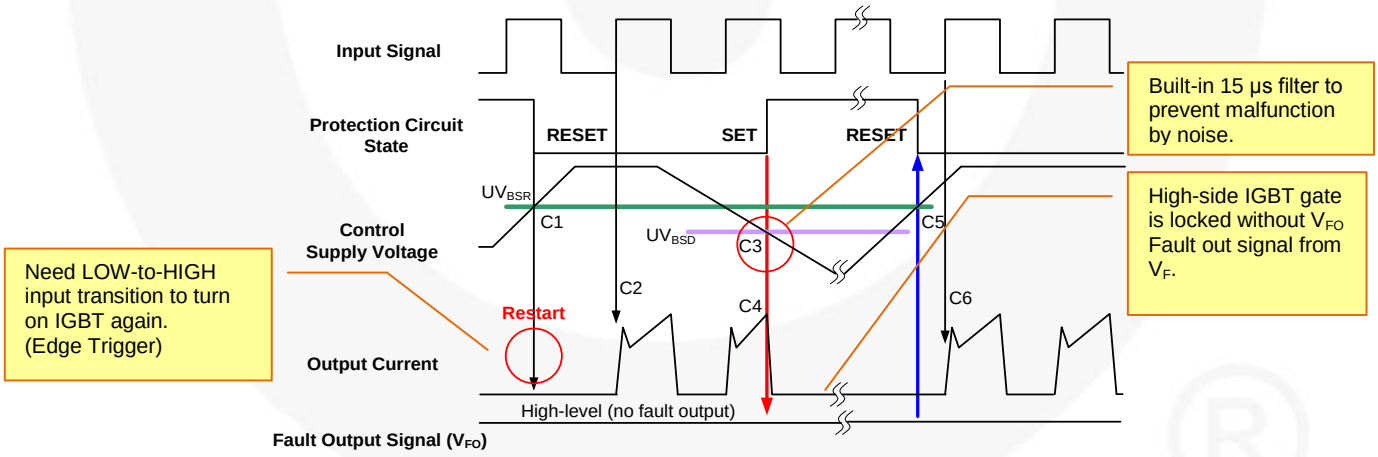


Figure 14. Timing Chart of High-Side Under-Voltage Protection Function

Notes:

24. C1-control supply voltage rises: after the voltage reaches UV_{BSR}, the circuit starts when the next input is applied.
25. C2-normal operation: IGBT ON and carrying current.
26. C3-under-voltage detection (UV_{BSD}).
27. C4-IGBT OFF in spite of control input is alive, but there is no fault output signal.
28. C5-under-voltage reset (UV_{BSR}).
29. C6-normal operation: IGBT ON and carrying current.

5. Key Parameter Design Guidance

For stable operation, there are recommended parameters for passive components and bias conditions, considering operating characteristics of Motion SPM® 45 V3 series.

5.1 Shunt Resistor Selection at N-Terminal for Current Sensing & Protection

The external RC time constant from the N-terminal shunt resistor to C_{SC} must be lower than 2 µs when overload condition is detected for a stable shutdown.

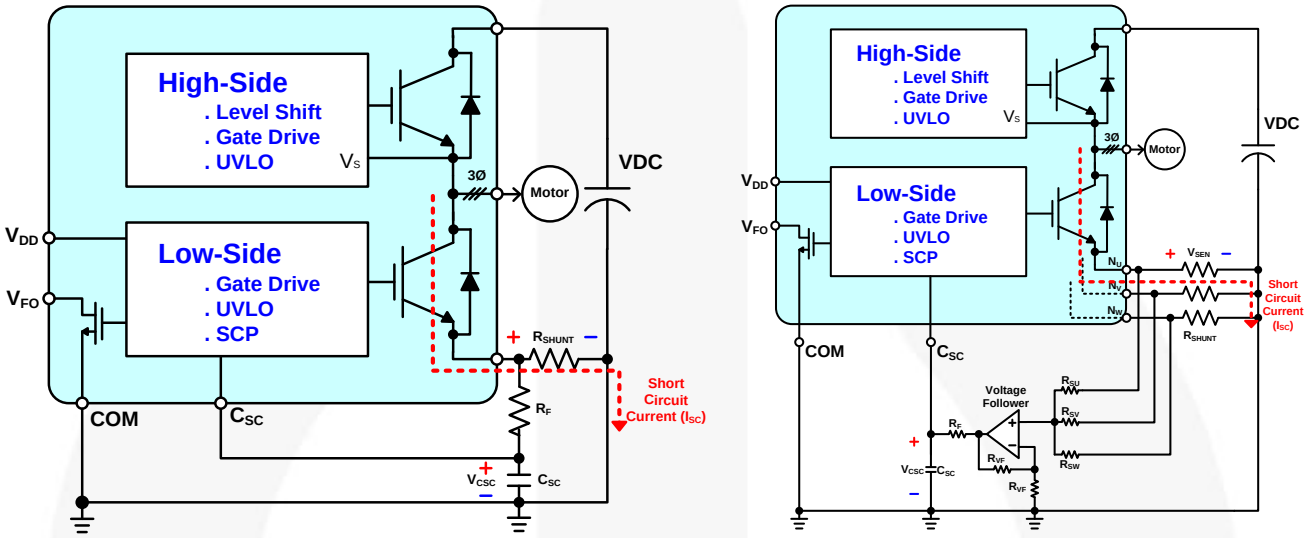


Figure 15. Recommended Circuitry for Over-Current Protection

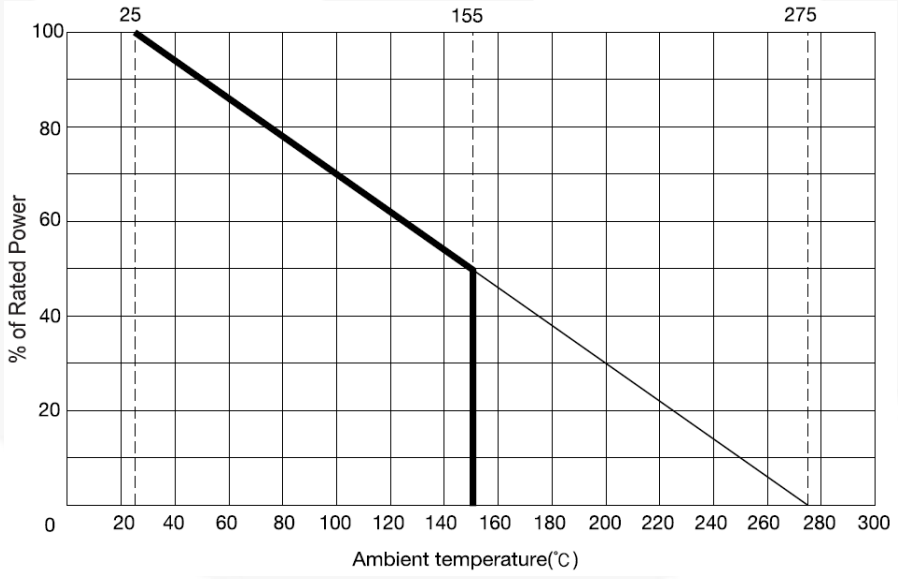


Figure 16. Derating Curve Example of Shunt Resistor (from RARA ELEC.)

Table 12. OCP & SCP Level ($V_{SC(ref)}$) Specification

Conditions	Min.	Typ.	Max.	Unit
Specification at T_J=25°C, V_{DD}=15 V	0.45	0.50	0.55	V

Table 13. Operating Over Current Range (R_{SHUNT}=12.2 mΩ (Min.), 12.8 mΩ (Typ.), 13.4 mΩ (Max.)) *(see the equations below)*

Conditions	Min.	Typ.	Max.	Unit
Operating SC Level at T_J=25°C	34	39	45	A

In case of one shunt, the value of shunt resistor is calculated by the following equations.

Maximum current trip level (depends on user selection):

$$I_{SC(max)} = 1.5 \times I_{C(max)}$$

SC trip reference voltage (depends on datasheet):

$$V_{SC(ref)} = min.\ 0.45\ V,\ typ.\ 0.5\ V,\ max.\ 0.55V$$

Shunt resistance:

$$I_{SC(max)} = V_{SC(max)} / R_{SHUNT(min)} \rightarrow R_{SHUNT(min)} = V_{SC(max)} / I_{SC(max)}$$

If the deviation of the shunt resistor is limited below ± 5%:

$$R_{SHUNT(typ)} = R_{SHUNT(min)} / 0.95,$$

$$R_{SHUNT(max)} = R_{SHUNT(typ)} \times 1.05$$

Actual SC trip current level becomes:

$$I_{SC(typ)} = V_{SC(typ)} / R_{SHUNT(typ)},\ I_{SC(min)} = V_{SC(min)} / R_{SHUNT(max)}$$

Inverter output power:

$$P_{OUT} = \frac{\sqrt{3}}{\sqrt{2}} \times MI \times V_{DC\_Link} \times I_{RMS} \times PF$$

where:

MI = Modulation Index;

V_{DC_Link} *= DC link voltage;*

I_{RMS} *= Maximum load current of inverter; and*

PF = Power Factor

Average DC current

$$I_{DC\_AVG} = V_{DC\_Link} / (P_{out} \times Eff)$$

where:

Eff = Inverter efficiency

The power rating of shunt resistor is calculated by the following equation:

$$P_{SHUNT} = (I^2_{DC\_AVG} \times R_{SHUNT} \times Margin) / Derating\ Ratio$$

where:

RSHUNT=Shunt resistor typical value at T_C*=25*°C

Derating Ratio=Derating ratio of shunt resistor at T_{SHUNT}*=100*°C

(From datasheet of shunt resistor); and

Margin = Safety margin (determined by user)

✓ **Shunt Resistor Calculation Examples**

Calculation Conditions:

- DUT: FNB43060Tx
- Tolerance of shunt resistor: ±5%
- SC Trip Reference Voltage:

  $V_{SC(min)}$=0.45 V, $V_{SC(typ)}$=0.50 V, $V_{SC(max)}$=0.55 V
- Maximum Load Current of Inverter (I_{RMS}): 15 A_{rms}
- Maximum Peak Load Current of Inverter ($I_{C(max)}$): 30 A
- Modulation Index (MI): 0.9
- DC Link Voltage (V_{DC_Link}): 300 V
- Power Factor (PF): 0.8
- Inverter Efficiency (Eff): 0.95
- Shunt Resistor Value at T_C = 25°C (R_{SHUNT}): 25 mΩ
- Derating Ration of Shunt Resistor at T_{SHUNT} = 100°C: 70% *(refer to Figure 16)*
- Safety Margin: 20%
- Calculation Results:
- $I_{SC(max)}$: 1.5 × $I_{C(max)}$ = 1.5 x 30 A = 45 A
- $R_{SHUNT(min)}$: $V_{SC(max)}$ / $I_{SC(max)}$=0.55 V / 45 A=12.2 mΩ
- $R_{SHUNT(typ)}$: $R_{SHUNT(min)}$ / 0.95 = 12 mΩ / 0.95 = 12.8 mΩ
- $R_{SHUNT(max)}$: $R_{SHUNT(typ)}$ x 1.05 = 40.0 mΩ x 1.05 = 13.4 mΩ
- $I_{SC(min)}$: $V_{SC(min)}$ / $R_{SHUNT(max)}$ = 0.45 V / 13.4 mΩ = 33.6 A
- $I_{SC(typ)}$: $V_{SC(typ)}$ / $R_{SHUNT(typ)}$ = 0.5 V / 12.8 mΩ = 39 A
- $P_{OUT} = \frac{\sqrt{3}}{\sqrt{2}} \times MI \times V_{DC\_Link} \times I_{RMS} \times PF = \frac{\sqrt{3}}{\sqrt{2}} \times 0.9 \times 300 \times 15 \times 0.8$ = 3968 W
- I_{DC_AVG} = (P_{OUT}/Eff) / V_{DC_Link} = 13.9 A
- P_{SHUNT} = ($I^2_{DC\_AVG}$ × R_{SHUNT} × Margin) / Derating Ratio = (7^2 × 0.026 × 1.2) / 0.7 = 4.24 W (Therefore, the proper power rating of shunt resistor is over 4.5 W)

5.2 Time Constant of Internal Delay

An RC filter prevents unexpected malfunction by noise-related signal like reverse recovery current of FWDi. The RC time constant is determined by the applied noise time and the Short-Circuit Current Withstanding Time (SCWT) of Motion SPM® 45 V3 series. When the R_{SHUNT} voltage exceeds the OCP level, this is applied to the C_{SC} pin via the RC filter. The RC filter delay (T1) is the time required for the C_{SC} pin voltage to rise to the referenced OCP level. The gate drive IC has an internal filter time (logic filter time for noise elimination: T2). Consider this filter time when designing the RC filter of V_{CSC}.

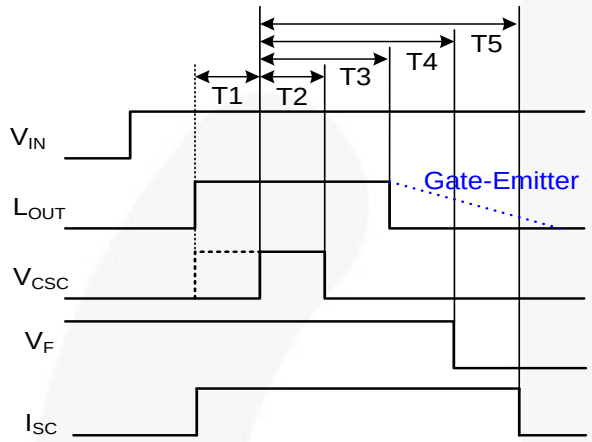


Figure 17. Timing Diagram

Notes:

30. V_{IN}: Voltage of input signal.
31. L_{OUT}: V_{GE} of low-side IGBT.
32. V_{CSC}: Voltage of C_{SC} pin.
33. I_{SC}: Over- or Short-circuit current.
34. V_F: Voltage of VF pin.
35. T1: filtering time of RC filter of V_{CSC}.
36. T2: filtering time of C_{SC}. If V_{CSC} width is less than T2, SCP does not operate.
37. T3: delay from C_{SC} triggering to gate-voltage down.
38. T4: delay from C_{SC} triggering to fault-out signal.
39. T5: delay from C_{SC} triggering to IGBT shutdown.

Table 14. Time Table on Short-Circuit Conditions: V_{CSC} to L_{OUT}, I_{SC}, V_F

Device Under Test	Typ. at T_J=25°C	Max. at T_J=25°C
FNB43060Tx	T2=0.4 µs	Considering ±20% Dispersion, T4=1.8 µs
	T3=0.6 µs	
	T4=1.5 µs	
	T5=1.3 µs	

Notes:

40. To guarantee safe short-circuit protection under all operating conditions, C_{SC} should be triggered within 0.4 µs after short-circuit occurs. (Recommendation: SCWT < 2.0 µs, Conditions: V_{DC}=400 V, V_{DD}=16.5 V, T_J=150°C).
41. It is recommended that delay from short-circuit to C_{SC} triggering should be minimized.

5.3 Soft Turn-Off

A soft turn-off function protects the low side IGBTs from over voltage of V_{PN} (supply voltage) by "hard off at over current or short circuit mode," which is when IGBTs are turned off by input signal before the OCP function under short-circuit condition. In this case, V_{PN} rapidly rises by fast and large di/dt of I_C (over-current or short-circuit current). This kind of rapid rise of V_{PN} can cause destruction of IGBT by over-voltage. Soft-off function prevents IGBT rapid turning off by slow discharging of V_{GE} (gate-to-emitter voltage of IGBT).

An internal block diagram of low side and operation sequence of soft turn-off function are shown in Figure 18 and Figure 19. This function operates by two internal protection functions (UVLO and SCP). When the IGBT is turned off in normal conditions, gate drive IC turns off the IGBT immediately by turn-off gate signal ($IN_{(XL)}$) via gate driver block. Pre-driver turn-on output buffer of gate driver block, path ①. When the IGBT is turned off by a protection function, the gate driver is disabled by the protection function signal via output of protection circuit (disable output buffer, high-Z) and output of the protection circuit turn-on switch of the soft-off function. V_{GE} (IGBT gate-emitter voltage) is discharged slowly via circuit of soft-off (path ②).

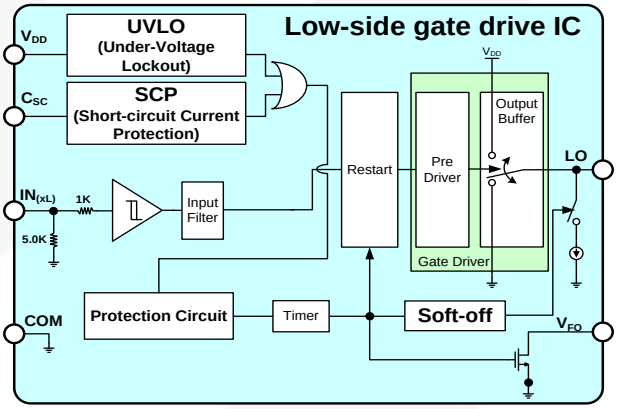


Figure 18. Internal Block Diagram of LS Gate Drive IC

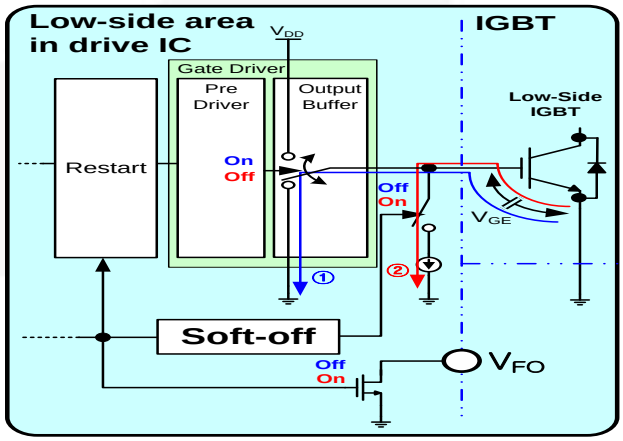


Figure 19. Operating Sequence of Soft Turn off

5.4 Fault Output Function

Because the V_{FO} terminal is an open-drain type, it should be pulled up to 3.3 V or 5 V via a pull-up resistor. The resistor has to satisfy the above specifications.

Table 15. Fault Output Maximum Ratings

Item	Symbol	Condition	Rating	Unit
Fault Output Voltage	V_{FO}	Applied between V_{FO}-COM	-0.3~V_{DD} +0.3	V
Fault Output Current	I_{FO}	Sink Current at V_{FO} Pin	1.0	mA

Table 16. Electric Characteristics

Item	Symbol	Condition	Min.	Max.	Unit
Fault Output Voltage	V_{FOH}	V_{SC}=0 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull-up	4.5		V
	V_{FOL}	V_{SC}=1 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull-up		0.5	V

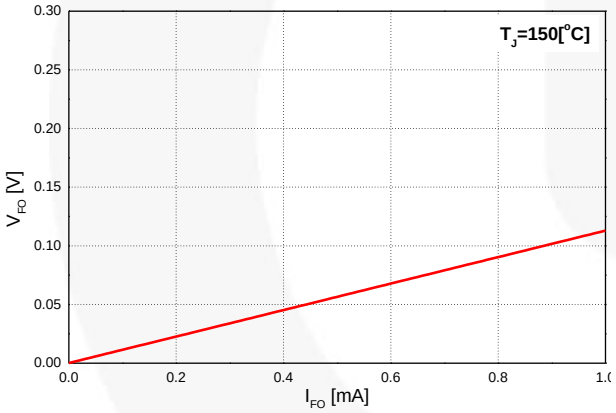


Figure 20. Voltage-Current Characteristics of V_{FO} Terminal

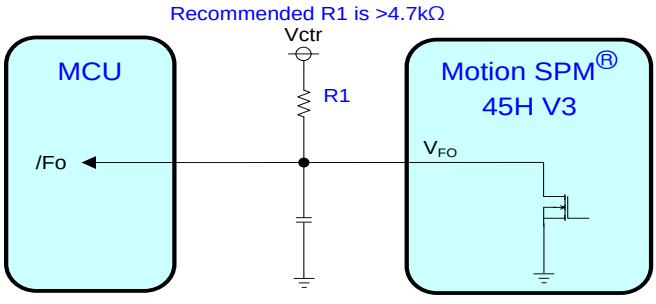


Figure 21. Proposed Circuit for Fault Output Function

5.5 Circuit of Input Signal (IN(xH), IN(xL))

0 shows the I/O interface circuit between the MCU and Motion SPM® 45 V3 series. Because the input logic of the Motion SPM® 45 V3 series is active HIGH and there are built-in pull-down resistors, external pull-down resistors are not needed.

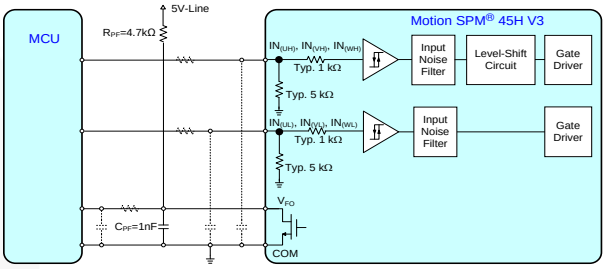


Figure 22. Recommended CPU I/O Interface Circuit

The input and fault output maximum rated voltages are shown in Table 17. Since the fault output is open drain, its rating is V_{DD} +0.3 V, 15 V supply interface is possible. However, it is recommended that the fault output be configured with the 5 V logic supplies, which is the same as the input signals. It is also recommended that the de-coupling capacitors be placed at both the MCU and Motion.

To avoid unexpected operation by fault signal, it is recommended to connect bypass capacitor to ends of the signal line for VFO pin and MCU as close as possible to each device. The RC coupling at each input (parts shown dotted in 0) can be changed depending on the PWM control scheme used in the application and the wiring impedance of the PCB layout.

The input signal section of the Motion SPM® 45 V3 series integrate 5 kΩ (typical) pull-down resistors. Therefore, when using an external filtering resistor between the MCU output and the Motion SPM® 45 V3 series input, attention should be given to the signal voltage drop at the Motion SPM® 45 V3 series input terminals to satisfy the turn-on threshold voltage requirement. For instance, R=100 Ω and C=1 nF can be used for the parts shown dotted in 0.

Table 17. Maximum Ratings of Input and VF Pins

Symbol	Item	Condition	Rating	Unit
V_{IN}	Input Signal Voltage	Applied between $IN_{(xH)}$, $IN_{(xL)}$-COM	-0.3 ~ V_{DD} +0.3	V

Table 18. Input Threshold Voltage Ratings (V_{DD}=15 V, T_J=25°C)

Symbol	Item	Condition	Min.	Max.	Unit
$V_{IN(ON)}$	Turn-On Threshold Voltage	$IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$-COM		2.6	V
$V_{IN(OFF)}$	Turn-Off Threshold Voltage	$IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$-COM	0.8		V

5.6 Bootstrap Circuit Design

5.6.1. Operation of Bootstrap Circuit

The V_{BS} voltage, which is the voltage difference between V_B (U, V, W) and V_S (U, V, W), provides the supply to the HVIC within the Motion SPM® 45 V3 series. This supply must be in the range of 13.0 V~18.5 V to ensure that the HVIC can fully drive the high-side IGBT. The under-voltage lockout protection for V_{BS} ensures that the HVIC does not drive the high-side IGBT if the V_{BS} voltage drops below a specific voltage (*refer to the datasheet of SPM® 45 series*). This function prevents the IGBT from operating in a high-dissipation mode.

There are a number of ways in which the V_{BS} floating supply can be generated. One of them is the bootstrap method described here (refer to Figure 23). This method has the advantage of being simple and inexpensive. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. SPM® 45 V3 series provide integrated bootstrap circuitry in driver. The bootstrap supply is formed by a combination of bootstrap diode, resistor, the current flow path of the bootstrap circuit is show in Figure 23. When V_S is pulled down to ground (low-side IGBT turn-on or low-side FWDi freewheeling), the bootstrap capacitor (C_{BS}) is charged through the integrated bootstrap diode from the V_{DD} supply.

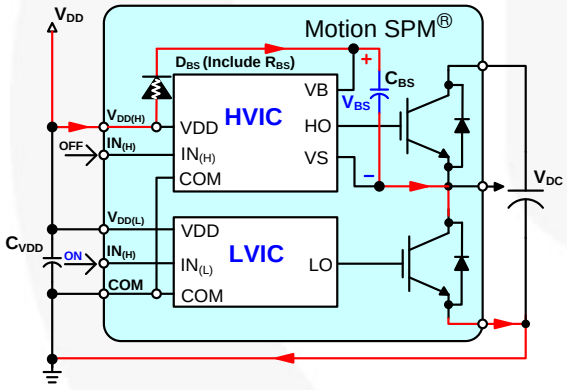


Figure 23. Current Path of Bootstrap Circuit to Charge C_{BS} when Low-Side IGBT Turns On

5.6.1. Selection of Bootstrap Capacitor Considering Initial Charging

Adequate on-time duration of the low-side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated from the following equation:

$$t_{charge} = C_{BS} \times R_{BS} \times \frac{1}{\delta} \times In \frac{V_{DD}}{V_{DD} - V_{BS(min)} - V_F - V_{LS}} \quad (1)$$

where:
V_F = forward voltage drop across the bootstrap diode;
$V_{BS(min)}$ = minimum value of the bootstrap capacitor;
V_{LS} = voltage drop across the low-side IGBT or load; and
δ = duty ratio PWM.

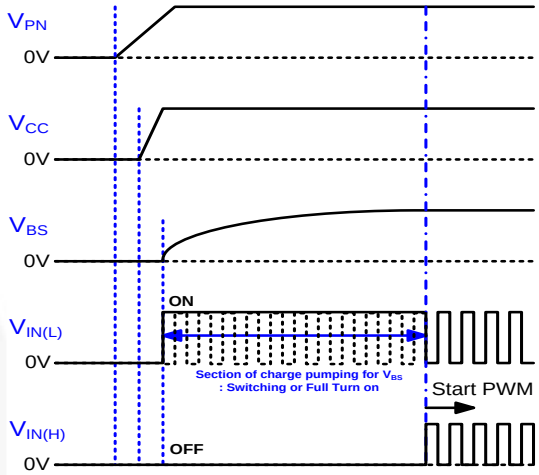


Figure 24. Timing Chart of Initial Bootstrap Charging

Enough on-time duration of the low-side IGBT to fully charge the bootstrap capacitor is initially required before normal operation of PWM starts for the Motion SPM® 45 V3 series. I-V characteristics of integrated bootstrap diode is shown in Figure 25 and recommended C_{BS} initial charging time (t_{charge}) is shown in Figure 26.

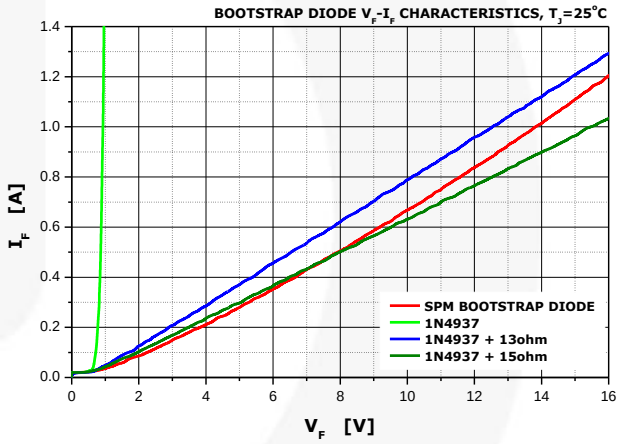


Figure 25. V-I Characteristics of Bootstrap Diode in Motion SPM® 45 V3 Series

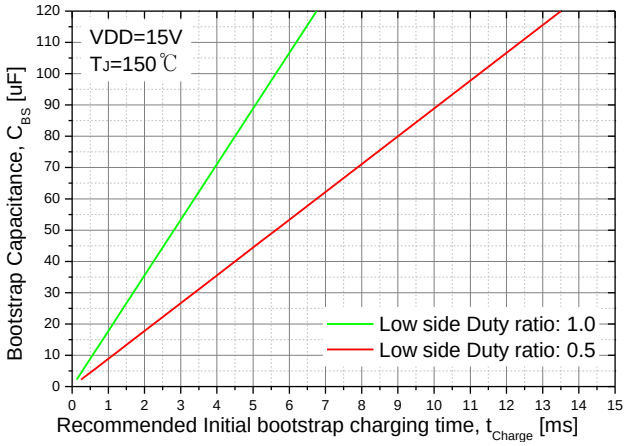


Figure 26. Recommended t_{charge} by C_{BS} and Duty Ratio

5.6.2. Selection of Bootstrap Capacitor Considering Operating

The bootstrap capacitance can be calculated by:

$$C_{BS} = \frac{I_{Leak} \times \Delta t}{\Delta V_{BS}} \quad (2)$$

where:
Δt = maximum on pulse width of high-side IGBT;
ΔV_{BS} = the allowable discharge voltage of the C_{BS} (voltage ripple); and
I_{Leak} = maximum discharge current of the C_{BS}.

Mainly via the following mechanisms:

- Gate charge for turning the high-side IGBT on…
- Quiescent current to the high-side circuit in the HVIC
- Level-shift charge required by level-shifters in HVIC
- Leakage current in the bootstrap diode
- C_{BS} capacitor leakage current (ignored for non-electrolytic capacitors)
- Bootstrap diode reverse recovery charge.

Practically, 2 mA of I_{Leak} is recommended for Motion SPM® 45 series. By taking consideration of dispersion and reliability, the capacitance is generally selected to be 2~3 times of the calculated one. The C_{BS} is only charged when the high-side IGBT is off and the V_S voltage is pulled down to ground. Therefore, the on-time of the low-side IGBT must be sufficient to ensure that the charge drawn from the C_{BS} capacitor can be fully replenished. Hence, there is an inherent minimum on-time for the low-side IGBT (or off-time of the high-side IGBT).

Calculation Examples of Bootstrap Capacitance A;

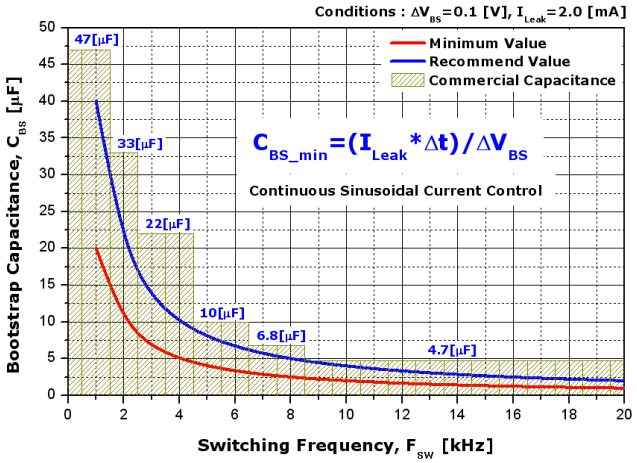


Figure 27. Capacitance of Bootstrap Capacitor on Variation of Switching Frequency

I_{Leak} = 2.0 mA (recommendation value)

ΔV_{BS} = 0.1 V (recommendation value)

Δt = 0.2 ms (depends on user system)

$$C_{BS\_min} = \frac{I_{Leak} \times \Delta t}{\Delta V_{BS}} = \frac{2mA \times 0.2ms}{0.1V} = 4.0 \times 10^{-6} \quad (3)$$

→ More than 2~3 times → 8 μF.

Note:

42. This capacitance value can be changed according to the switching frequency, capacitor used, and recommended V_{BS} voltage of 13.0~18.5 V (from datasheet). The above result is just a calculation example. This value can be changed according to the actual control method and lifetime of component.

Calculation Examples of Bootstrap Capacitance B;

The appropriate value for bootstrap capacitors should be selected based on operating conditions, UV_{BS} function, and allowable recommended $V_{B(X)}$-$V_{S(X)}$.

To avoid unexpected under-voltage protection and to keep V_{BS} within recommended value, bootstrap capacitance should be selected based on the operating conditions. Bootstrap voltage ripple is influenced by bootstrap resistor, load condition, output frequency, and switching frequency. Check the bootstrap voltage under the maximum load condition in the system. Figure 28 shows example of $V_{B(X)}$-$V_{S(X)}$ ripple voltage during operation.

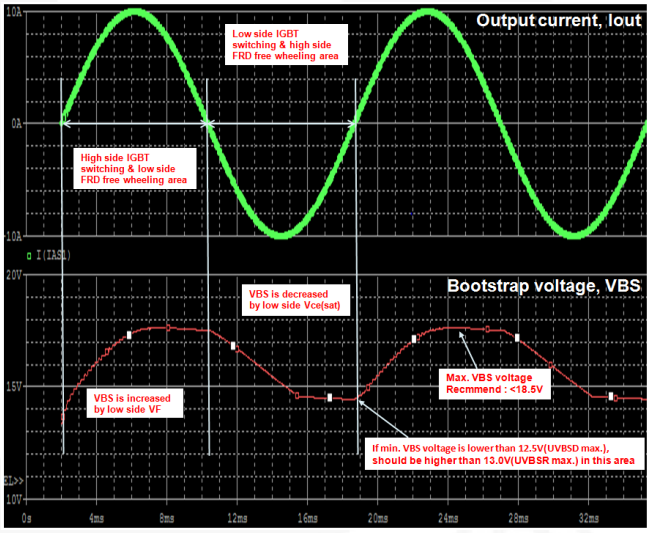


Figure 28. Recommendation of Bootstrap Ripple Voltage during Operation

5.6.3. Circuit of NTC Thermistor (Monitoring of T_C)

The Motion SPM® 45 series includes a Negative Temperature Coefficient (NTC) thermistor for module case temperature (T_C) sensing. This thermistor is located in ceramic substrate with the power chip (IGBT/FWDi). Therefore, the thermistor can accurately reflect the temperature of the power chip *(see Figure 29)*.

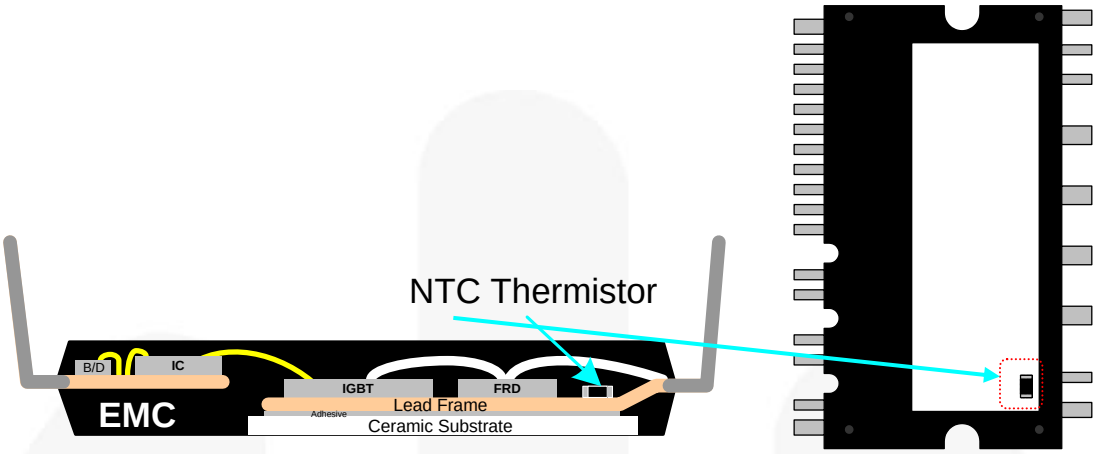


Figure 29. Location of NTC Thermistor in Motion SPM® 45 Series Package

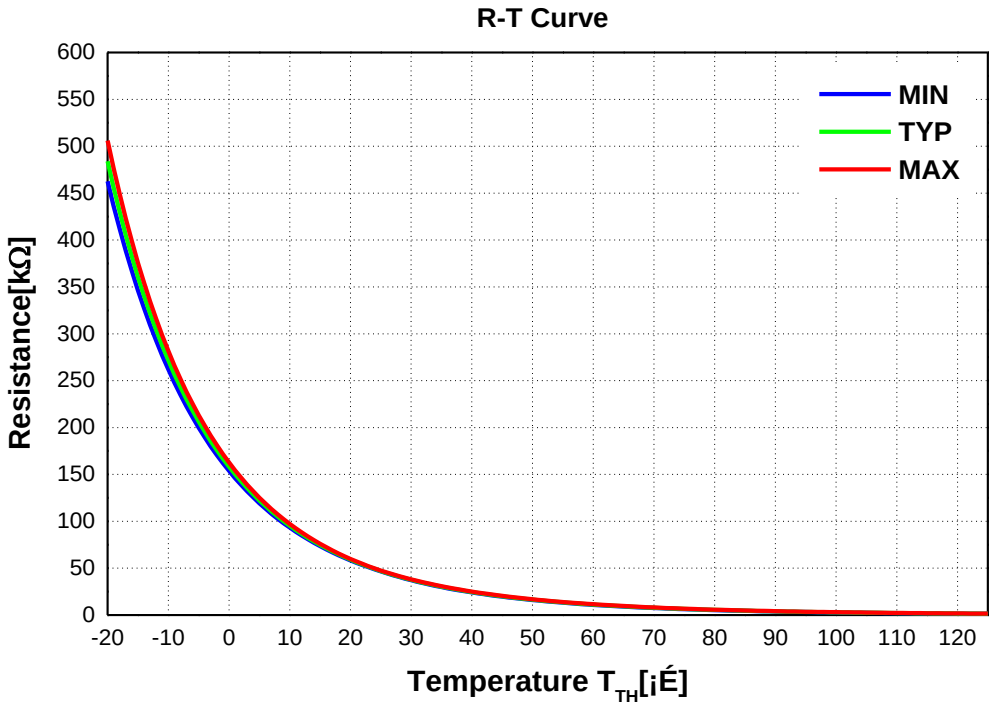


Figure 30. R-T Curve of NTC Thermistor in SPM45H Package

Normally, circuit designers use two kinds of circuit for temperature protection (monitoring) by NTC thermistor. One is circuit by Analog-Digital Converter (ADC).

The other is circuit by comparator. Figure 31 and Figure 32 show examples of application circuits with an NTC thermistor.

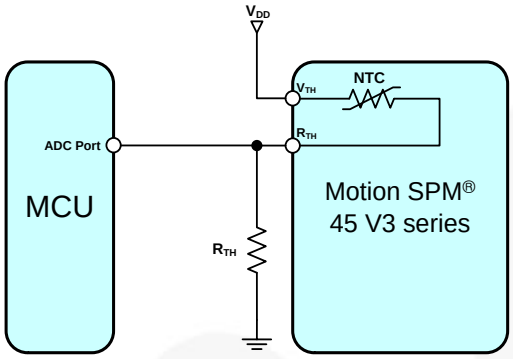


Figure 31. Over-Temperature Protection Circuit by MCU with NTC Thermistor

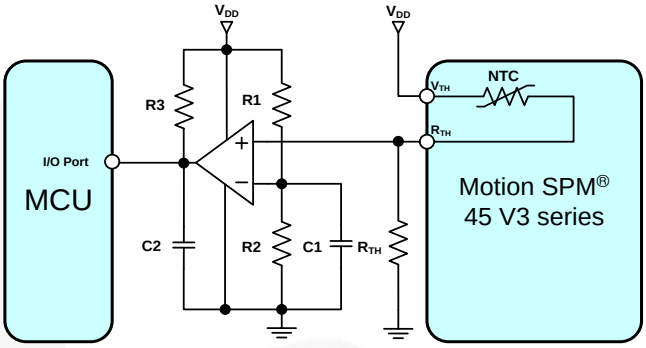


Figure 32. Over-Temperature Protection Circuit by Comparator with NTC Thermistor

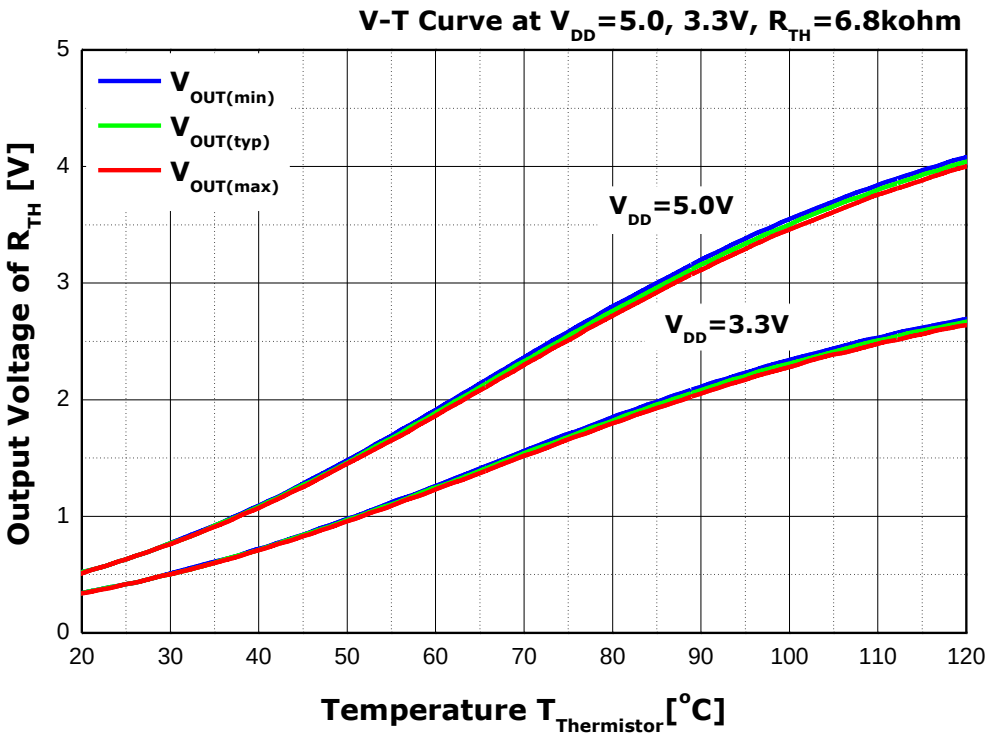


Figure 33. V-T Curve of Figure 31

Table 19. R-T Table of NTC Thermistor (1-1)]

TNTC(°C)	Rmin(kΩ)	Rcent(kΩ)	Rmax(kΩ)	T(°C)	Rmin(kΩ)	Rcent(kΩ)	Rmax(kΩ)
0	153.8063	158.2144	162.7327	30	37.1428	37.6431	38.1463
1	146.0956	150.1651	154.3326	31	35.5329	36.0351	36.5408
2	138.8168	142.5725	146.4152	32	34.0011	34.5041	35.0111
3	131.9431	135.4081	138.9502	33	32.5433	33.0462	33.5534
4	125.4497	128.6453	131.9091	34	31.1555	31.6573	32.1640
5	119.3135	122.2594	125.2655	35	29.8340	30.3339	30.8392
6	113.5129	116.2273	118.9947	36	28.5760	29.0734	29.5764
7	108.0276	110.5275	113.0739	37	27.3776	27.8717	28.3720
8	102.8388	105.1398	107.4814	38	26.2356	26.7260	27.2228
9	97.9288	100.0454	102.1974	39	25.1472	25.6332	26.1261
10	93.2812	95.2267	97.2031	40	24.1094	24.5907	25.0792
11	88.8803	90.6673	92.4810	41	23.1198	23.5960	24.0796
12	84.7119	86.3519	88.0148	42	22.1759	22.6466	23.1249
13	80.7624	82.2661	83.7894	43	21.2753	21.7401	22.2129
14	77.0190	78.3963	79.7903	44	20.4158	20.8746	21.3416
15	73.4700	74.7302	76.0043	45	19.5953	20.0478	20.5088
16	70.1042	71.2558	72.4189	46	18.812	19.2580	19.7126
17	66.9112	67.9620	69.0224	47	18.0638	18.5032	18.9514
18	63.8812	64.8386	65.8039	48	17.3492	17.7818	18.2234
19	61.0050	61.8759	62.7530	49	16.6663	17.0921	17.5269
20	58.2739	59.0647	59.8601	50	16.0137	16.4325	16.8605
21	55.6798	56.3961	57.1160	51	15.3899	15.8016	16.2227
22	53.2152	53.8628	54.5127	52	14.7934	15.1981	15.6122
23	50.8732	51.4569	52.0422	53	14.2230	14.6205	15.0277
24	48.6469	49.1715	49.6969	54	13.6773	14.0677	14.4678
25	46.5300	47.0000	47.4700	55	13.1552	13.5385	13.9316
26	44.4567	44.936	45.4159	56	12.6556	13.0318	13.4178
27	42.4868	42.9737	43.4618	57	12.1774	12.5465	12.9255
28	40.6147	41.1075	41.6021	58	11.7195	12.0815	12.4536
29	38.8351	39.3323	39.8319	59	11.2810	11.6361	12.0011
30	37.1428	37.6431	38.1463	60	10.8610	11.2091	11.5673

Table 20. R-T Table of NTC Thermistor (1-2)

TNTC(°C)	Rmin(kΩ)	Rcent(kΩ)	Rmax(kΩ)	T(°C)	Rmin(kΩ)	Rcent(kΩ)	Rmax(kΩ)
61	10.4594	10.8007	11.1520	91	3.6675	3.8463	4.0334
62	10.0746	10.4091	10.7536	92	3.5505	3.7253	3.9084
63	9.7058	10.0336	10.3714	93	3.4377	3.6087	3.7879
64	9.3522	9.6734	10.0046	94	3.3290	3.4963	3.6716
65	9.0133	9.3279	9.6525	95	3.2242	3.3878	3.5593
66	8.6882	8.9963	9.3145	96	3.1235	3.2836	3.4515
67	8.3764	8.6782	8.9899	97	3.0264	3.1830	3.3473
68	8.0773	8.3727	8.6782	98	2.9328	3.0860	3.2468
69	7.7902	8.0795	8.3787	99	2.8425	2.9923	3.1497
70	7.5147	7.7979	8.0910	100	2.7553	2.9019	3.0559
71	7.2496	7.5268	7.8138	101	2.6712	2.8146	2.9654
72	6.9950	7.2663	7.5474	102	2.5901	2.7303	2.8779
73	6.7505	7.0160	7.2913	103	2.5117	2.6489	2.7933
74	6.5157	6.7755	7.0450	104	2.4360	2.5703	2.7117
75	6.2901	6.5443	6.8082	105	2.3630	2.4943	2.6327
76	6.0739	6.3227	6.5810	106	2.2921	2.4206	2.556
77	5.8662	6.1096	6.3624	107	2.2236	2.3493	2.4819
78	5.6665	5.9046	6.1521	108	2.1575	2.2805	2.4102
79	5.4745	5.7075	5.9498	109	2.0936	2.2139	2.3409
80	5.2899	5.5178	5.7549	110	2.0319	2.1496	2.2739
81	5.1129	5.3358	5.5680	111	1.9725	2.0877	2.2094
82	4.9426	5.1607	5.3879	112	1.9151	2.0278	2.1470
83	4.7788	4.9921	5.2145	113	1.8596	1.9699	2.0866
84	4.6211	4.8299	5.0475	114	1.8060	1.9139	2.0282
85	4.4694	4.6736	4.8866	115	1.7541	1.8598	1.9716
86	4.3228	4.5226	4.7310	116	1.7042	1.8076	1.9171
87	4.1817	4.3771	4.5811	117	1.6559	1.7572	1.8644
88	4.0459	4.2369	4.4366	118	1.6092	1.7083	1.8134
89	3.9150	4.1019	4.2973	119	1.5640	1.6611	1.7639
90	3.7890	3.9717	4.1629	120	1.5203	1.6153	1.7161

5.7 General Application Circuit Example

Figure 34 shows a general application circuitry of interface schematic with control signals connected directly to an MCU.

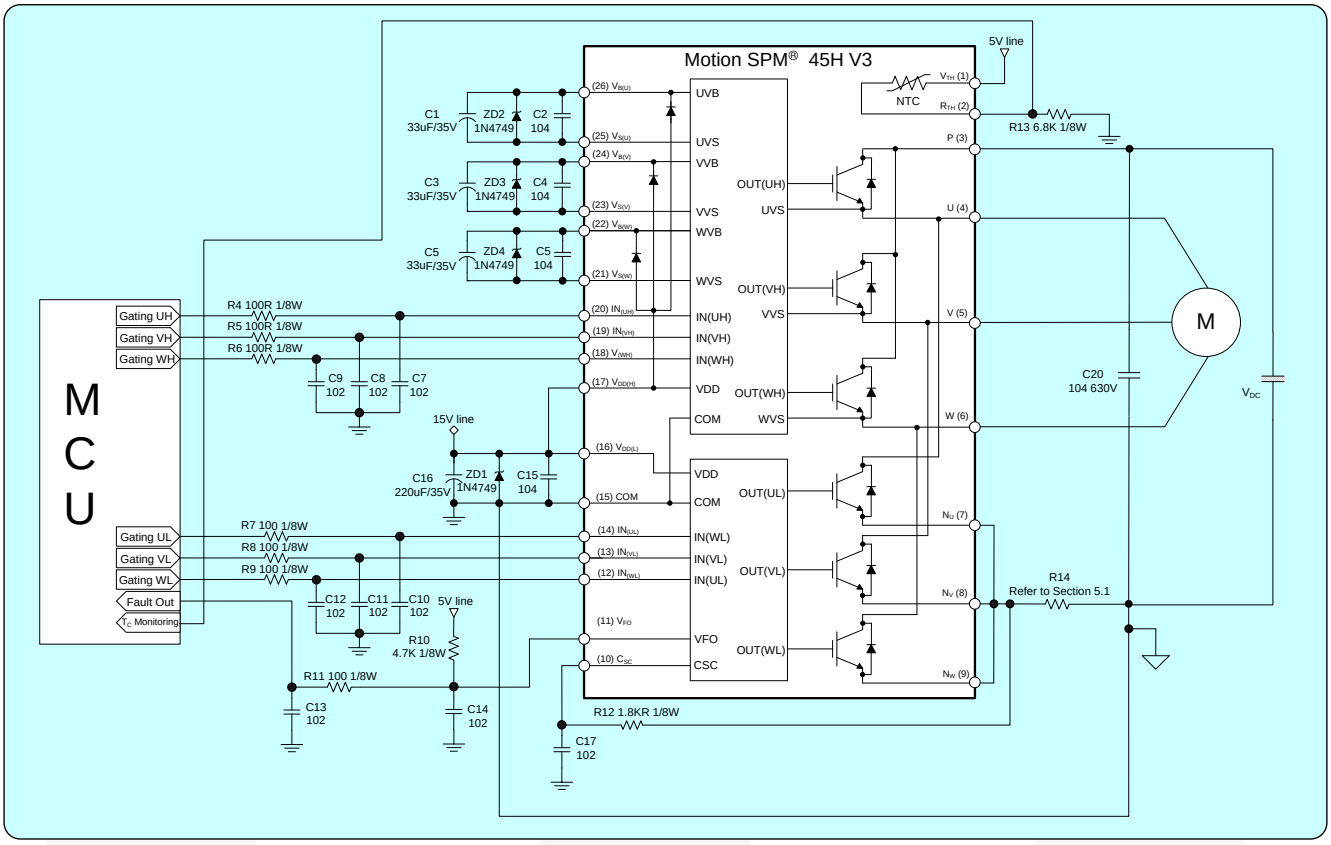


Figure 34. General Application Circuitry for Motion SPM® 45 V3 Series (One-SHUNT Solution)

5.8 Print Circuit Board (PCB) Layout Guidance

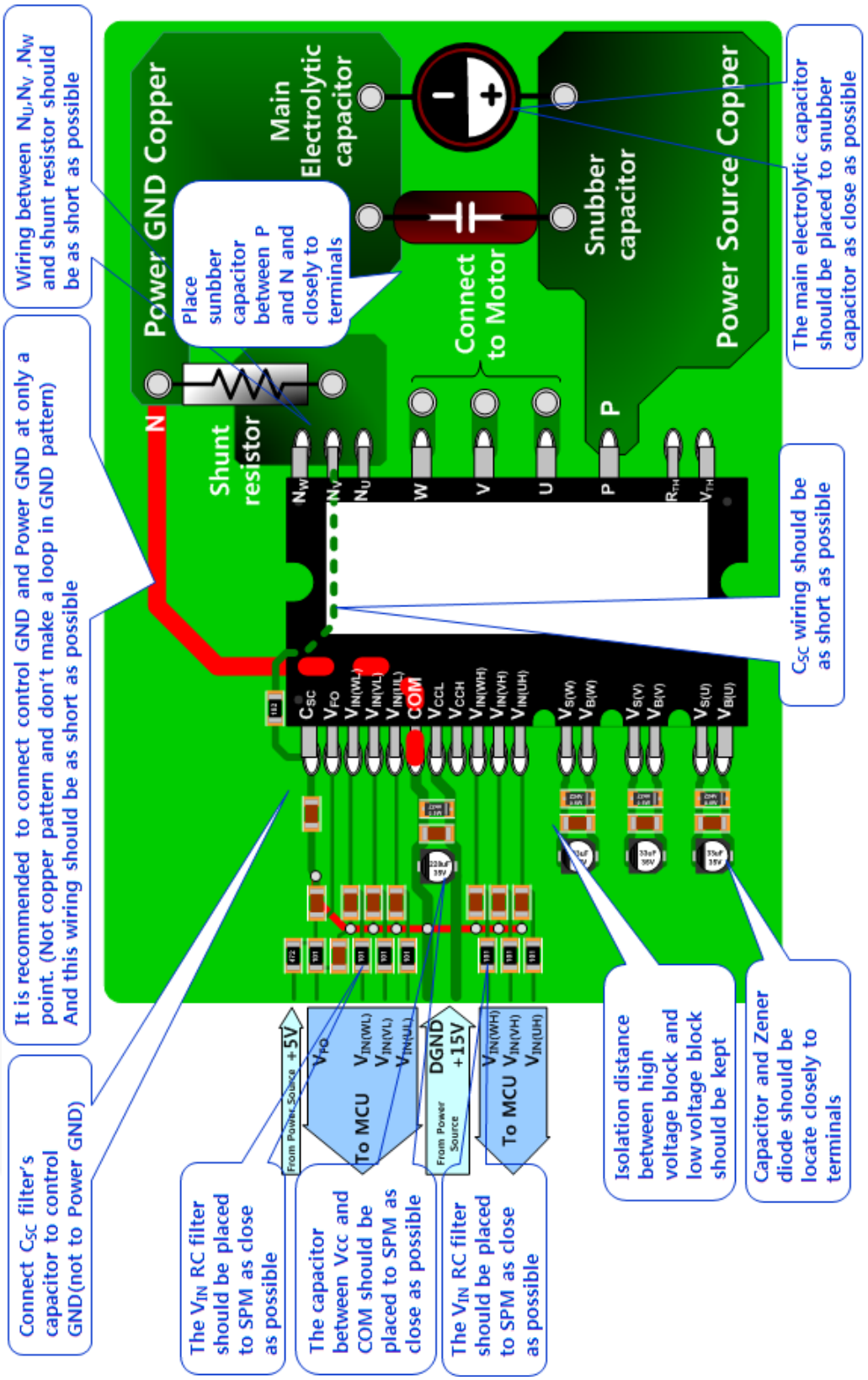
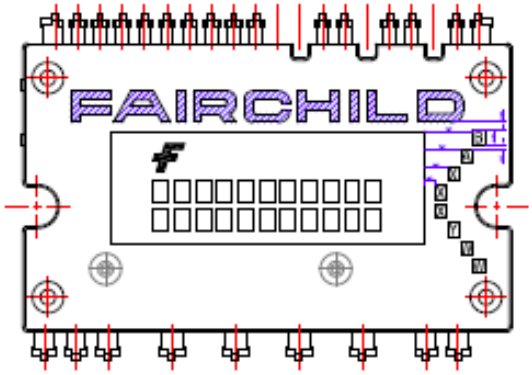


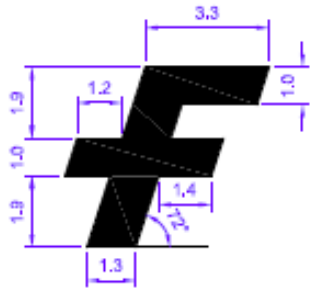
Figure 35. PCB Layout Guidance

6. Marking Information

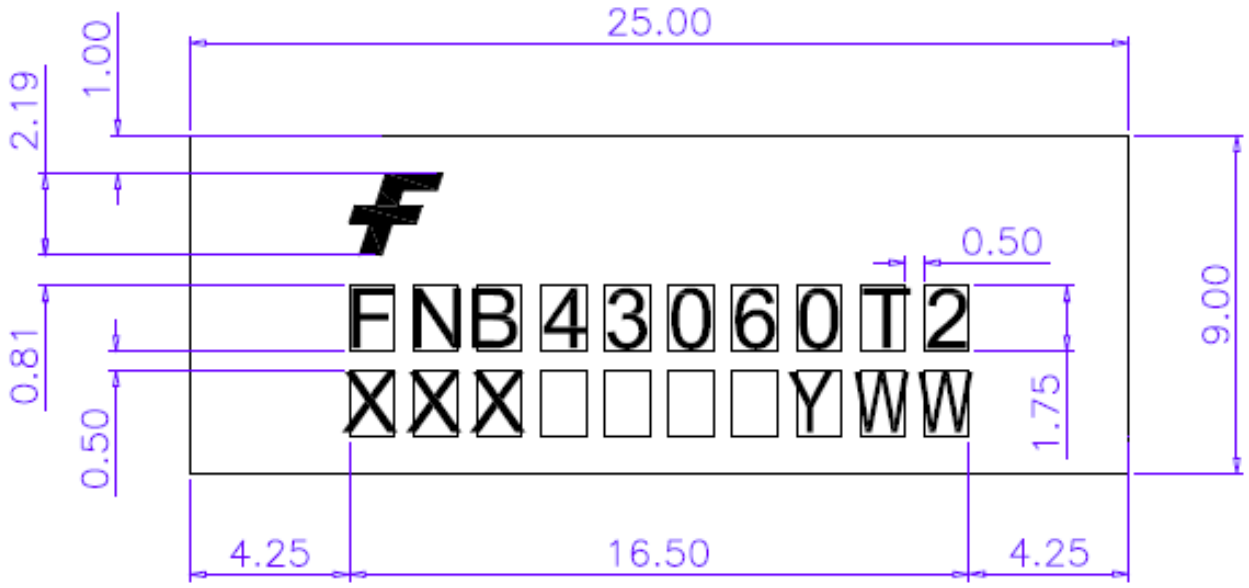
* MARKING LAY-OUT



FAIRCHILD SEMICONDUCTOR LOGO
DIMENSIONAL PROPORTION



* MARKING DIMENSION



Y	Alphabet
2010	A
2011	B
2012	C
2013	D
2014	E
2015	F
2016	G
2017	H
2018	J
2019	K
2020	A

* NOTE

1. F : FAIRCHILD LOGO
2. XXX : LAST 3 DIGITS OF LOT NO(OPTION CODE)
3. YWW : WORK WEEK CODE ("Y" REFERS TO THE RIGHT ALPHABET CHARACTER TABLE)
4. Hole Side Marking :
   -,BA ; FNB43060T2(Product name)
   -, XXX : Last 3 digits of Lot No.
   -, YWW : Work Week Code("Y" Refers to the right alphabet character table)

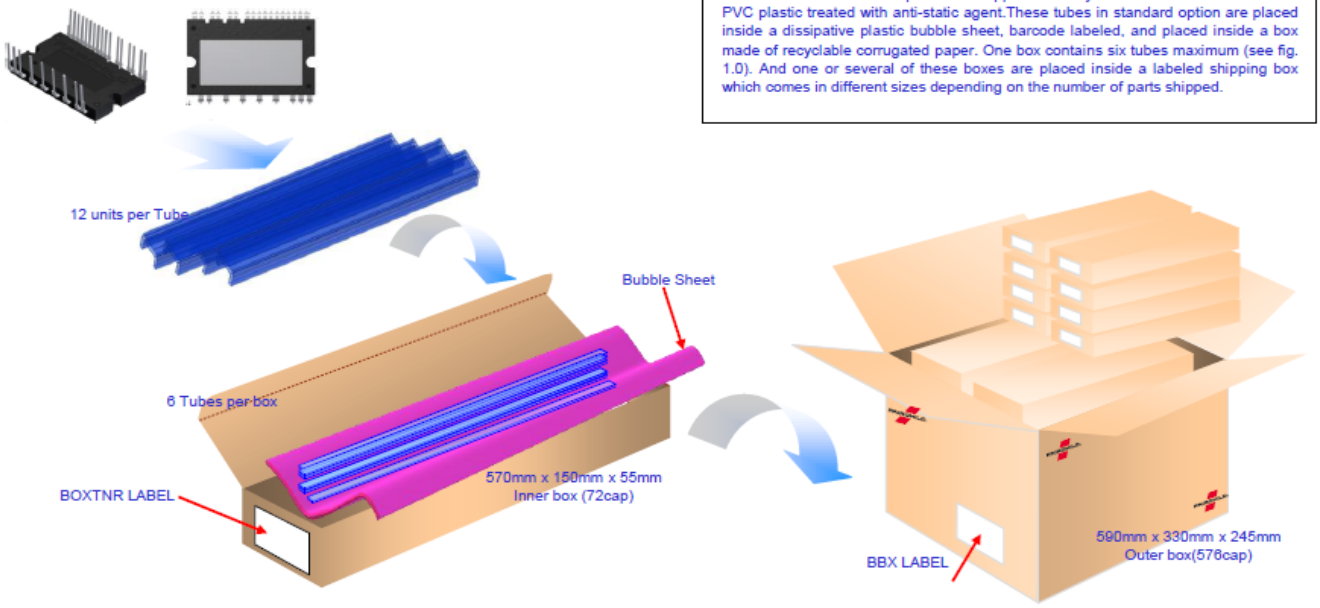
Figure 36. Marking Information

7. Packaging Specification

SPMAA-C26/SPMAB-C26 Tube Packing Configuration: Figure 1.0

Packaging Description:

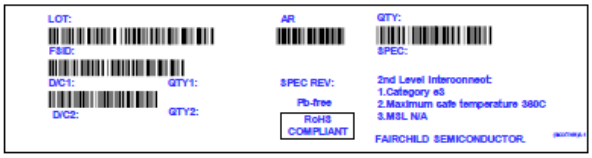
SPMAA-C26/SPMAB-C26 parts are shipped normally in tube. The tube is made of PVC plastic treated with anti-static agent.These tubes in standard option are placed inside a dissipative plastic bubble sheet, barcode labeled, and placed inside a box made of recyclable corrugated paper. One box contains six tubes maximum (see fig. 1.0). And one or several of these boxes are placed inside a labeled shipping box which comes in different sizes depending on the number of parts shipped.



SPMAA-C26/SPMAB-C26 Packaging Information: Figure 2.0

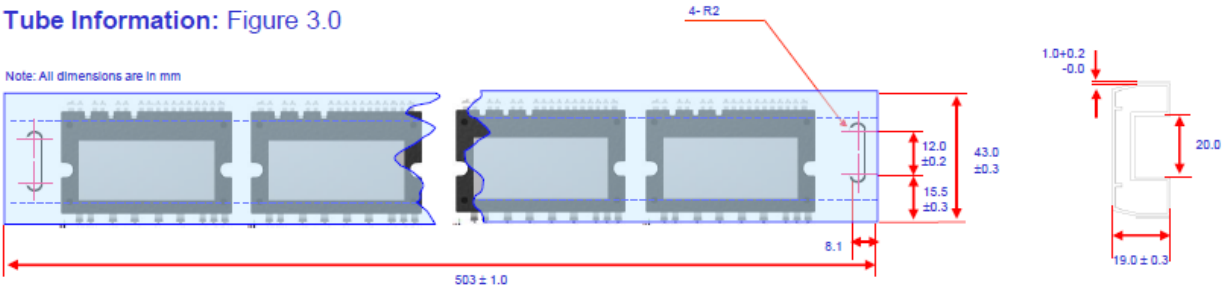
SPMAA-C26/SPMAB-C26 Packaging Information	
Packaging Option	Standard (no flow code)
Packaging type	Rail/Tube
Qty per Tube/ Inner Box	12
Inner Box Dimension (mm)	570x150x55
Max qty per Box	72
Outer Box Dimension (mm)	590x330x245
Max qty per Box	576

Inner Box Barcode Label Sample_(BOXTNR)



Outer Box Barcode Label Sample_(BBX)

SPMAA-C26/SPMAB-C26 Tube Information: Figure 3.0



NOTES:

A : ALL DIMENSION ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED

B : DRAWING FILE NAME : PKG-MOD26ACAREV3.0

Figure 37. SPMAx-C26 Packaging Specification

8. Related Resources

FNB43060Tx — Smart Power Module Motion SPM® 45 V3

AN-9072 — Smart Power Module Motion SPM® 45 Mounting Guidance

AN-9071 — Smart Power Module Motion SPM® 45 Thermal Performance Information

RD-344 — Reference Design for FNA41560 (One Shunt Solution)

RD-345 — Reference Design for FNA41560 (Three Shunt Solution)

Motion Control Design Tool at http://www.fairchildsemi.com/design_tools/motion_control_design_tool/

PUBLICATION ORDERING INFORMATION

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