NEC ELECTRON DEVICE ■ 6427525 0049601 488 ■NECE

MOS INTEGRATED CIRCUIT

μPD63200

18 BIT D/A CONVERTER

The μPD63200 is a 18-bit D/A converter for digital audio equipment.

Resistance strings system and built-in 0-point offset circuit realizes high sound quality. This CMOS LSI operates on +5 V single power supply with low current consumption.

FEATURES

- 18 bit resolution
- +5 V single power supply
- CMOS configuration
- Built-in output operational amplifier
- Built-in 0-point offset circuit
- Resistance strings system
- 8 f_s (2 channels x 400 kHz) capability
- Built-in 2 channel DAC
- Symmetrical phase output
- Input data format : 2's complement
  MSB First

ORDERING INFORMATION

Ordering Name	Package	Quality Grade
μPD63200GS	16-Pin Plastic SOP (300 mil)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

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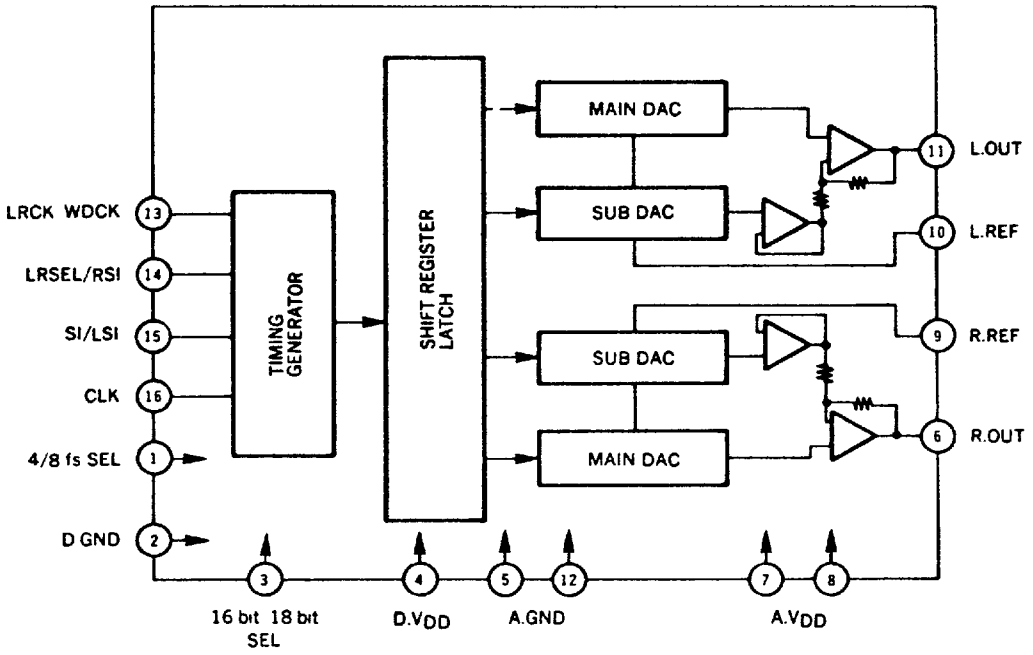
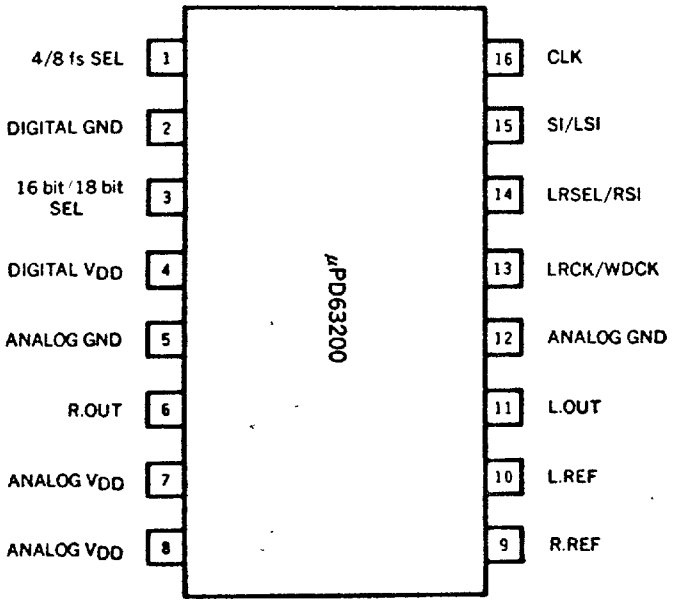
Date Published June 1992 M
Printed in Japan

BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}	−0.3 to +7.0	V
Output Voltage	V_{OUT}	−0.3 to V_{DD} +0.3	V
Input Voltage	V_{IN}	−0.3 to V_{DD} +0.3	V
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

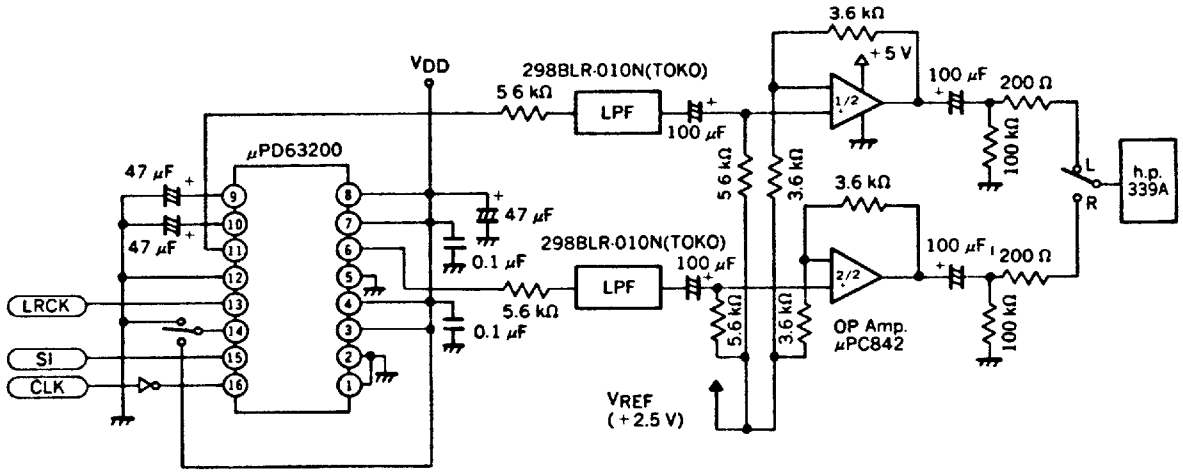
RECOMMENDED OPERATING RANGES

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
High-level Input Voltage	V_{IH}	0.7 V_{DD}		V_{DD}	V	
Low-level Input Voltage	V_{IL}	0		0.3 V_{DD}	V	
Ambient Temperature	T_a	−20	25	75	°C	
Load Resistance	R_L	5			kΩ	R.OUT, L.OUT terminal
Sampling Frequency	f_s			400	kHz	
Clock Frequency	f_{CLK}			10	MHz	
Clock Pulse Width	t_{SCK}	40			ns	
SI, LRCK Setup Time	t_{DC}	12			ns	
SI, LRCK Hold Time	t_{CD}	12			ns	

ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_{DD} = +5 V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Resolution	RES		18		bit	
Total Harmonic Distortion 1	THD_1		0.03	0.06	%	"A" RANK; f_{IN} = 1 kHz, 0 dB
				0.09		"B" RANK; f_{IN} = 1 kHz, 0 dB
Total Harmonic Distortion 2	THD_2		0.03	0.08	%	f_{IN} = 1 kHz, −5 dB
Total Harmonic Distortion 3	THD_3		0.035	0.18	%	f_{IN} = 1 kHz, −20 dB
Full Scale Output Voltage	V_{FS}		2.0		V_{p-p}	
Cross Talk	C.T	92	100		dB	One Side Channel 0 dB; f_{IN} = 1 kHz
S/N Ratio	S/N	100	105		dB	JIS-A
Dynamic Range	D.R	95	100		dB	f_{IN} = 1 kHz, −60 dB
Supply Current	I_{DD}		6.0	12	mA	f_{IN} = 1 kHz, 0 dB

TEST CIRCUIT

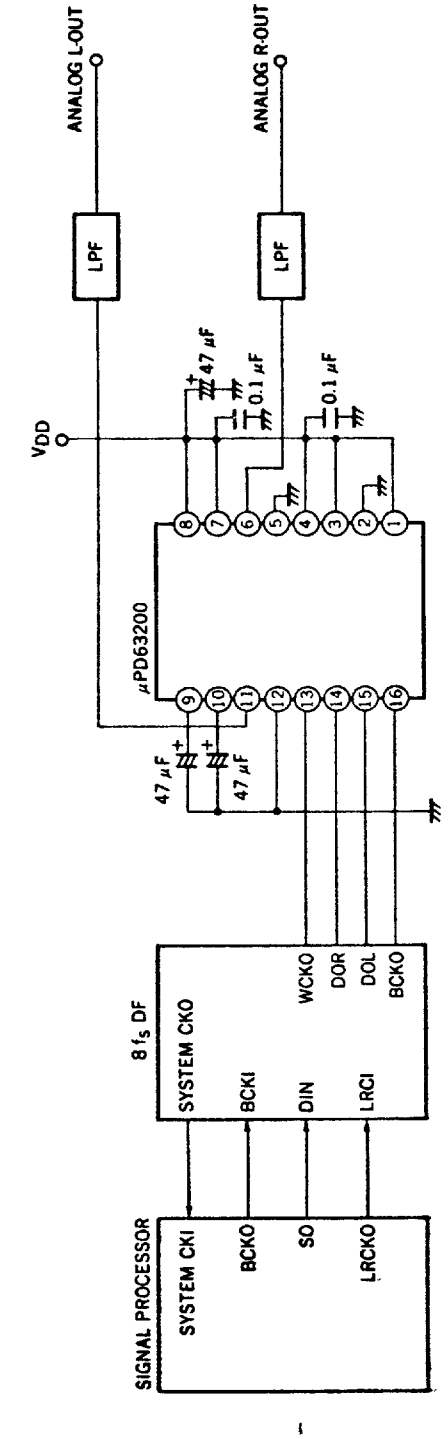


Sampling Frequency f_S = 88.2 kHz

TERMINAL FUNCTION

TERMINAL NO.	SYMBOL	TERMINAL NAME	DESCRIPTION	INPUT/ OUTPUT
1	4/8 f_s SEL	4/8 f_s Selection	As this terminal is "Low" or open, L-ch data and R-ch data are inputted for serial data by the pin 15. As this terminal is "High", L-ch data is inputted by the pin 15, R-ch data is inputted by the pin 14. (Pull-downed by the 100 kΩ resistance in IC.)	Input
2	D. GND	Digital GND	Ground terminal for the logic circuit	
3	16 bit/18 bit SEL	16 bit/18 bit Selection	As this terminal is "Low" or open, this IC operates as 16 bit D/A converter. As this terminal is "High", this IC operates as 18 bit D/A converter. (Pull-down by the 100 kΩ resistance in IC.)	Input
4	D. V_{DD}	Digital V_{DD}	Power supply terminal for the logic circuit	
5	A. GND	Analog GND	Ground terminal for the analog circuit	
6	R. OUT	R-ch OUTPUT	Output terminal for the right analog signal	Output
7	A. V_{DD}	Analog V_{DD}	Power supply terminal for the analog circuit	
8	A. V_{DD}	Analog V_{DD}		
9	R. REF	R-ch Voltage Reference	Operational Amplifier reference bias terminal. Normally connected to A. GND via a capacitor.	
10	L. REF	L-ch Voltage Reference		
11	L. OUT	L-ch OUTPUT	Output terminal for the left analog signal	Output
12	A. GND	Analog GND	Ground terminal for the analog circuit	
13	LRCK/WDCK	Left/Right Clock Word Clock	As the pin 1 is "Low" or open, this is input terminal for left/right identification signal. As the pin 1 is "High", this is input terminal for word identification signal of input data.	Input
14	LRSEL/RSI	Left/Right Selection R-ch Series Input	As the pin 1 is "Low" or open, this is left/right selection terminal for LRCK signal. At "High" of LRCK signal, set LRSEL pin at "Low" for L-ch DATA input. At "Low" of LRCK signal, set LRSEL pin at "High" for L-ch DATA input. As the pin 1 is "High", this is input terminal for R-ch serial data.	Input
15	SI/LSI	Series Input L-ch Series Input	As the pin 1 is "Low" or open, this is input terminal for L-ch and R-ch serial data. As the pin 1 is "High", this is input terminal for L-ch serial data.	Input
16	CLK	Clock	Input terminal for read clock of serial input data.	Input

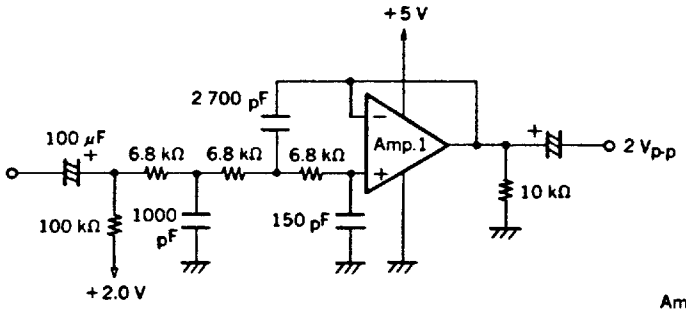
APPLICATION CIRCUIT



The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

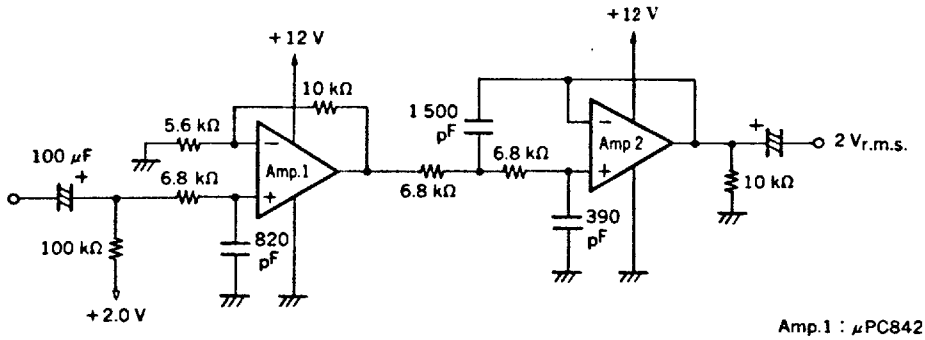
EXAMPLES OF OUTPUT LOW PASS FILTER

(1) In case that supply voltage is only +5 V.
(It is necessary to use a low satiation Operational amplifier as μPC842.)



Amp.1 : μPC842

(2) In case that the maximum amplitude of output voltage must be 2 $V_{r.m.s.(typ.)}$.
(It is necessary to use low satiation Operational amplifiers.)



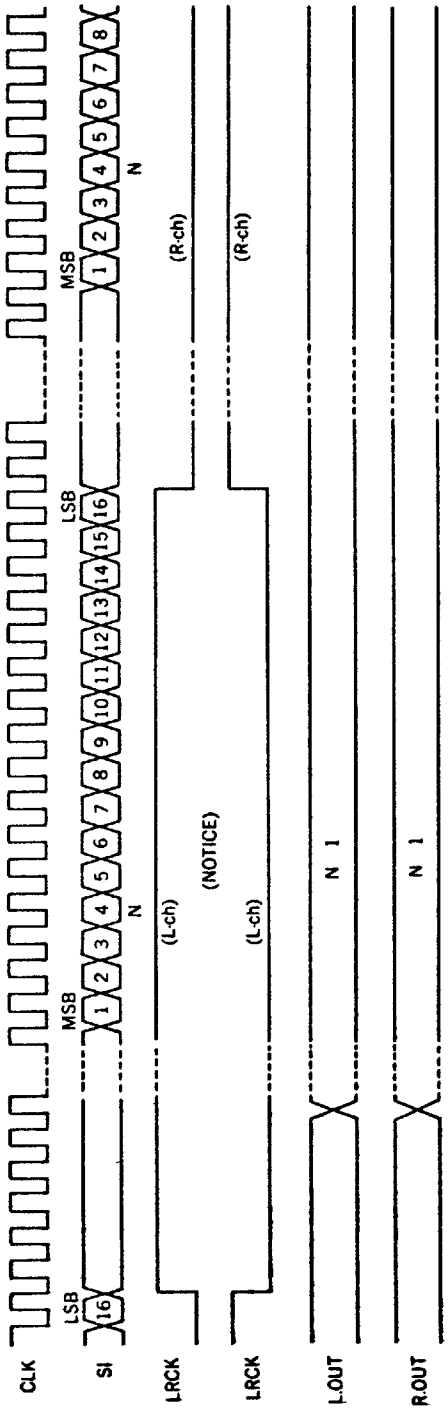
Amp.1 : μPC842
Amp.2 : μPC4572

TIMING CHART 1

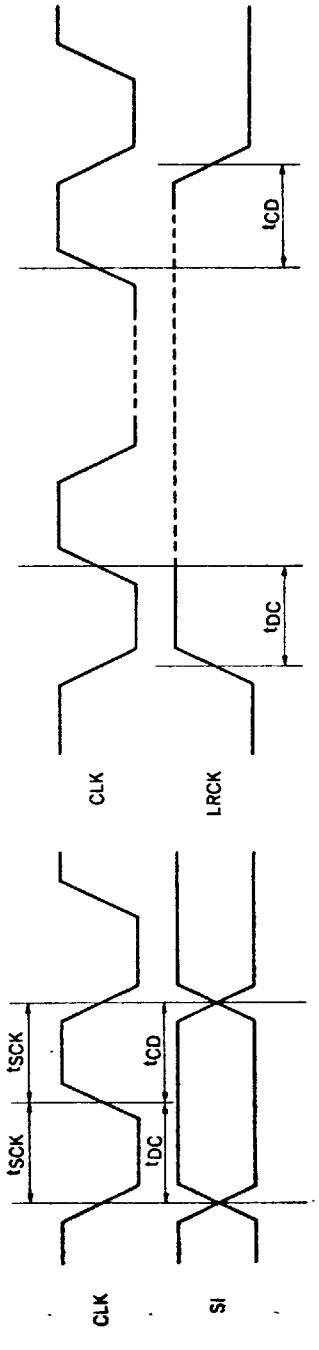
SELECTED MODE: 16 BIT DATA/SERIAL INPUT

SELECTED STATES OF TERMINALS

TERMINAL NAME	STATES
16 bit/18 bit SEL	Low (or open)
4/8 fs SEL	Low (or open)



(NOTICE) At "High" of LRCK signal, set LRSEL pin at "Low" for L-ch DATA input.
At "Low" of LRCK signal, set LRSEL pin at "High" for L-ch DATA input.

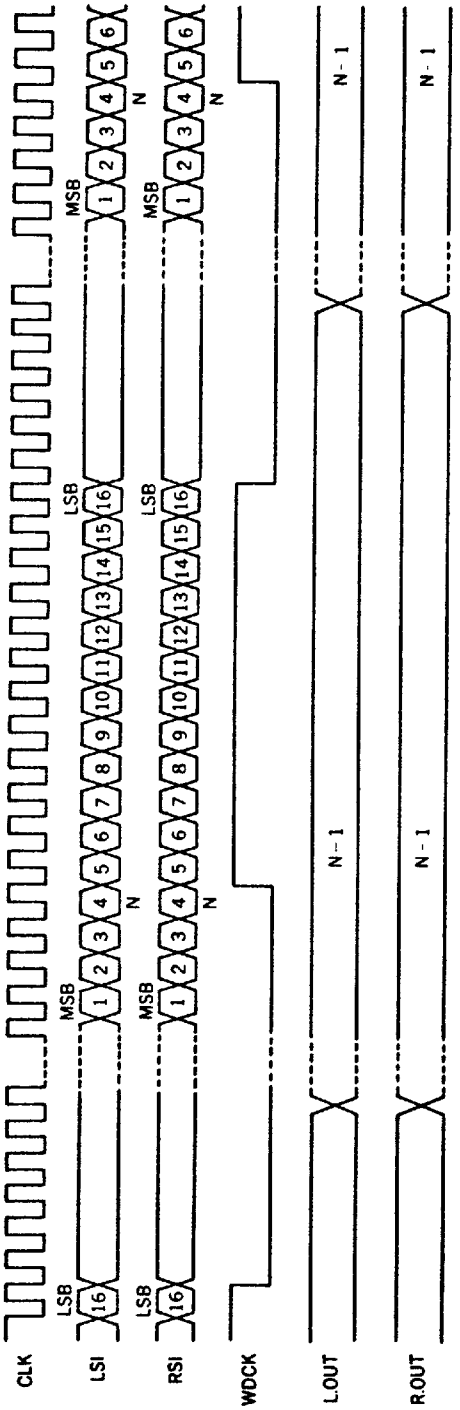


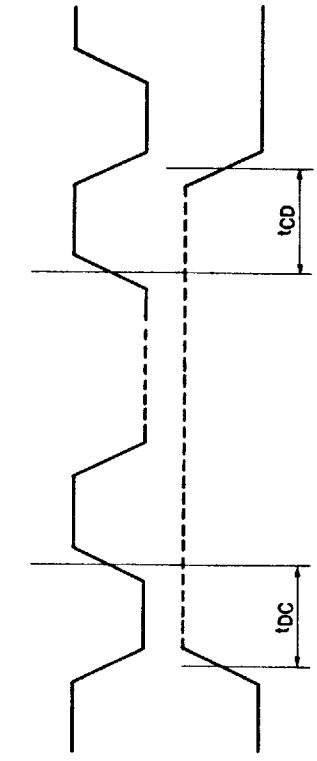
TIMING CHART 2

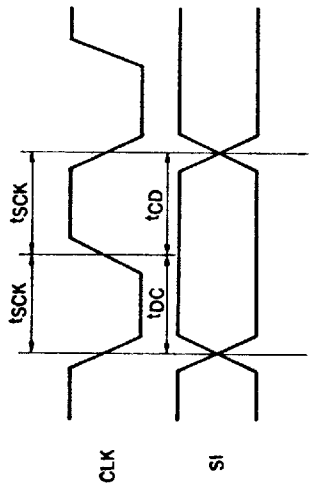
SELECTED MODE: 16 BIT DATA/PARALLEL INPUT

SELECTED STATES OF TERMINALS

TERMINAL NAME	STATES
16 bit/18 bit SEL	Low (or open)
4/8 fs SEL	High





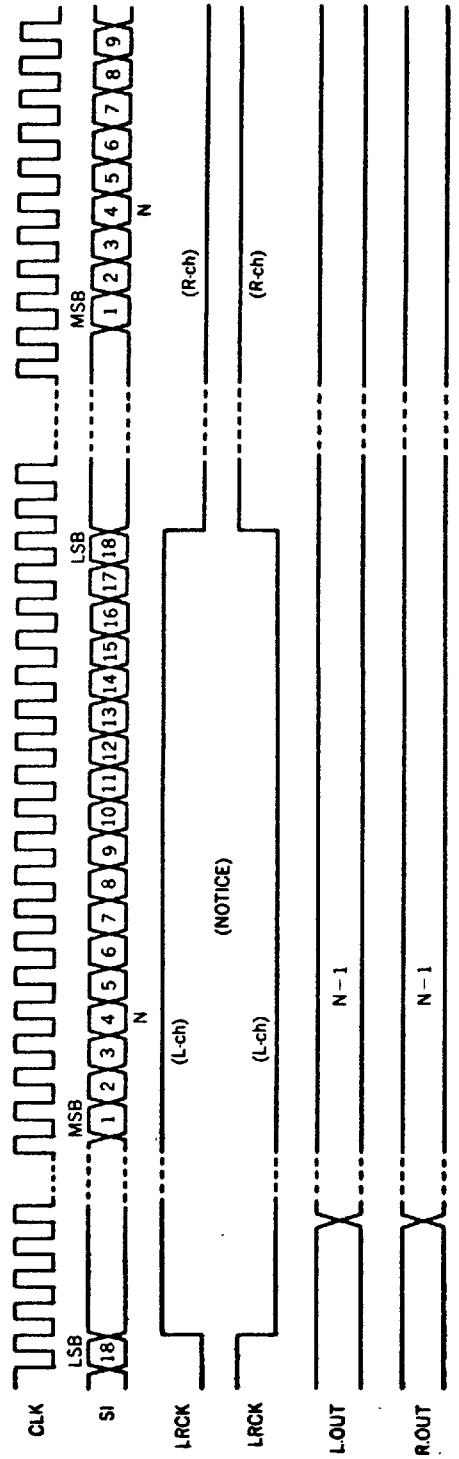


TIMING CHART 3

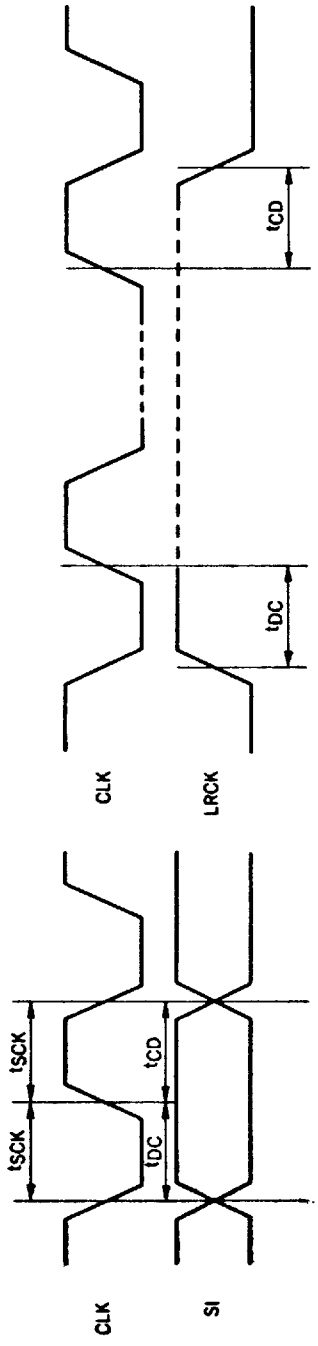
SELECTED MODE: 18 BIT DATA/SERIAL INPUT

SELECTED STATES OF TERMINALS

TERMINAL NAME	STATES
16 bit/18 bit SEL	High
4/8 fs SEL	Low (or open)



(NOTICE) At "High" of LRCK signal, set LRSEL pin at "Low" for L-ch DATA input.
At "Low" of LRCK signal, set LRSEL pin at "High" for L-ch DATA input.

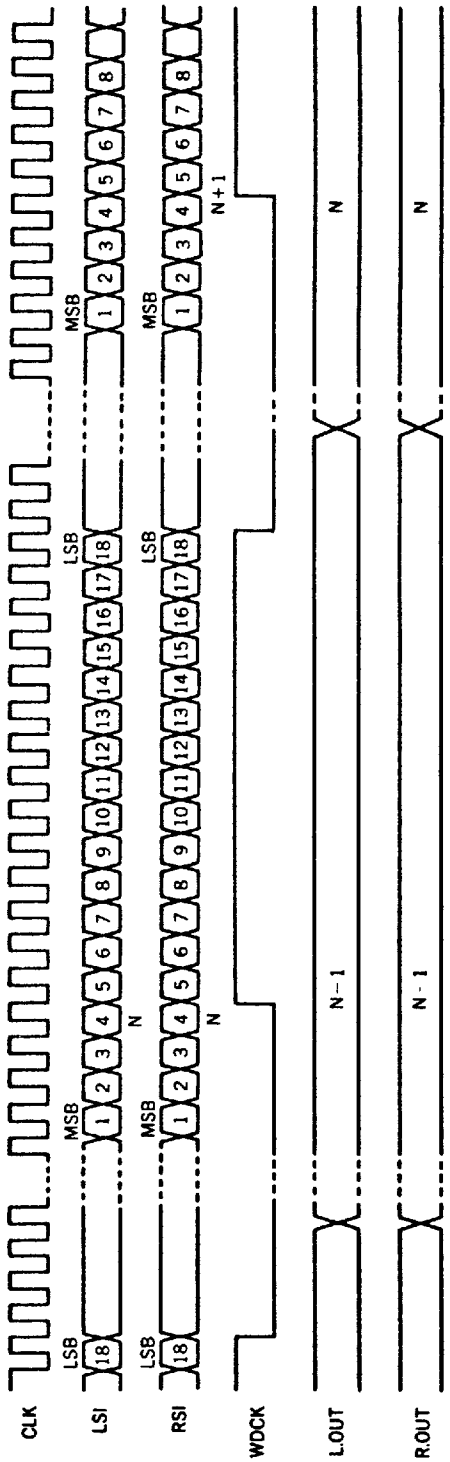


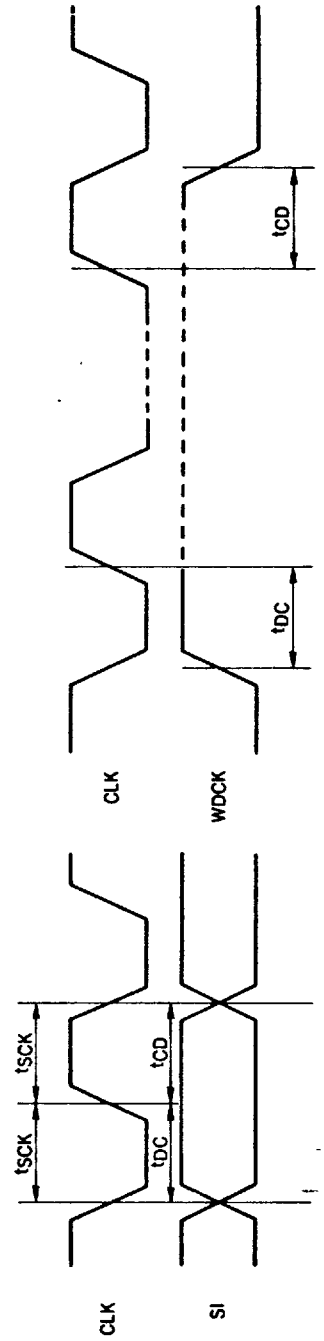
TIMING CHART 4

SELECTED MODE: 18 BIT DATA/PARALLEL INPUT

SELECTED STATES OF TERMINALS

TERMINAL NAME	STATES
16 bit/18 bit SEL	High
4/8 fs SEL	High





[EXPLANATION OF INPUT DATA FORMAT]

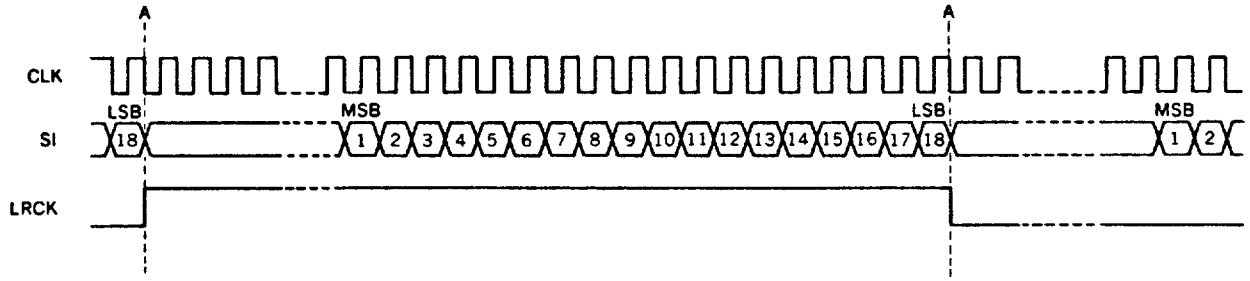
- MSB first
- Binary Two's Complementary
- SI, LSI, RSI, LRCK, and WDCK can turn over only when CLK gets down.

1. IN CASE THAT CLK IS CONTINUOUS

1.1 IN CASE THAT PIN 1 IS "LOW" OR OPEN

LRCK must turn over at the point "A" in Fig. 1.

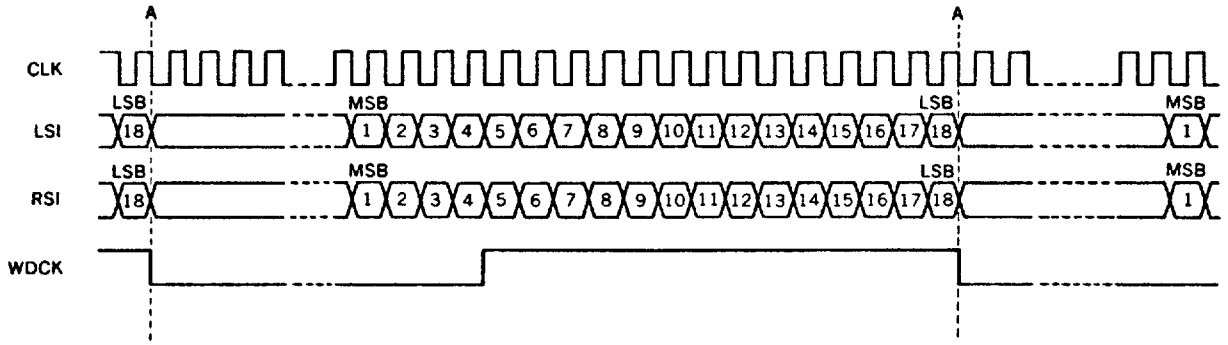
Fig. 1



1.2 IN CASE THAT PIN 1 IS "HIGH"

WDCK must get down at the point "A" in Fig. 2.

Fig. 2

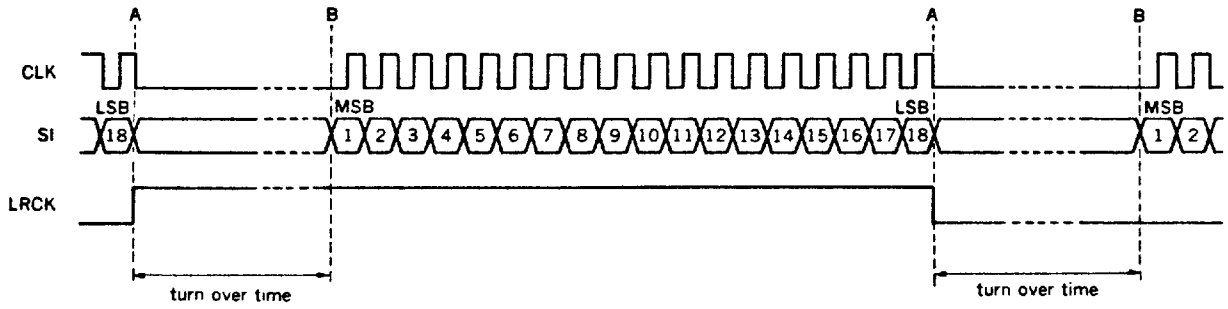


2. IN CASE THAT CLK IS CONTINUOUS ONLY WHEN SI IS INPUTTED.

2.1 IN CASE THAT PIN 1 IS "LOW" OR OPEN

LRCK must turn over at the point "A", at the point "B", or between the point "A" and the point "B" in Fig. 3.

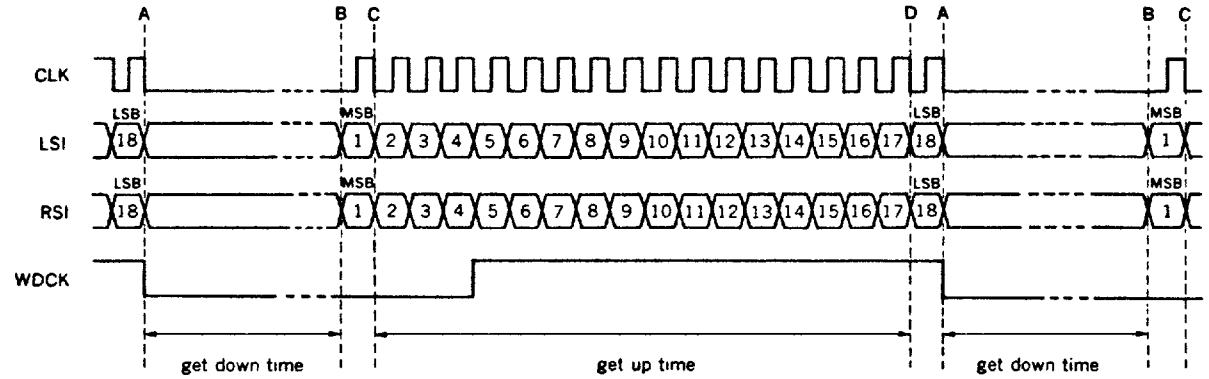
Fig. 3



2.2 IN CASE THAT PIN 1 IS "HIGH"

WDCK must get down at the point "A", at the point "B", or between the point "A" and the point "B" in Fig. 4.
And WDCK must get up at the point "C", at the point "D", or between the point "C" and the point "D" in Fig. 4.

Fig. 4



[NOTICE FOR USE]

Please attach muting circuits at the rear of μPD63200, or pop noise may be generated when the power is turned on.

[RECOMMENDED SOLDERING CONDITIONS]

The following conditions (see table below) must be met when soldering this product.
Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

<TYPE OF SURFACE MOUNT DEVICE>

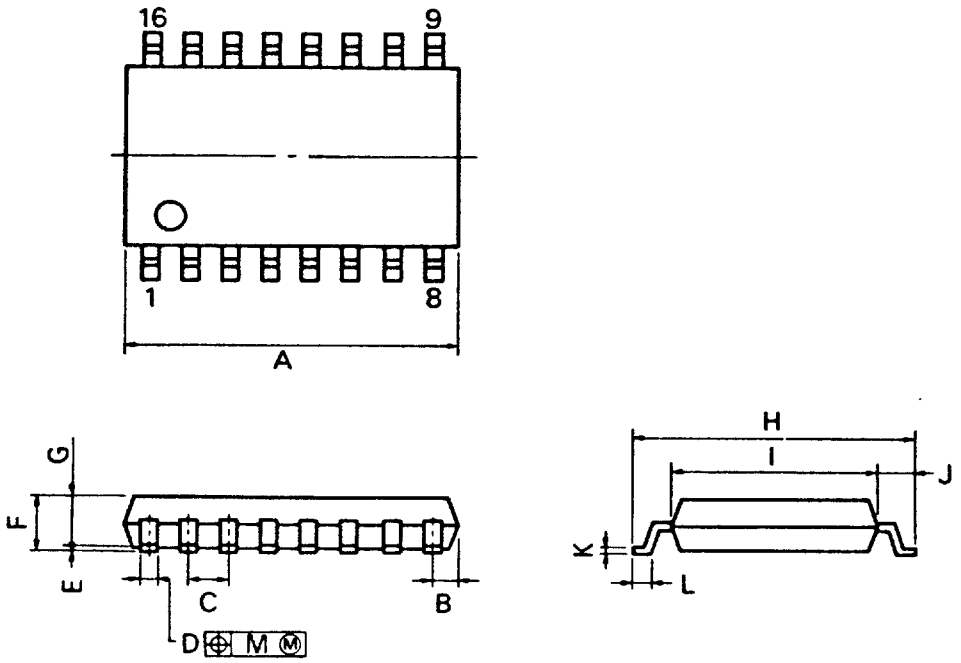
For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).
μPD63200GS

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C or below. Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 1, Exposure limit*: 3 days (10 hours pre-backing is required at 125 °C afterwards)	IR35-103-1
Partial heating method	Terminal temperature: 300 °C or below, Flow time: 10 seconds or below, Exposure limit*: None	

*: Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Note: Do not apply more than a single process at once, except for "Partial heating method".

16PIN PLASTIC SOP (300 mil)



P16GM-50-300B-1

ITEM	MILLIMETERS	INCHES
A	10.46 MAX.	0.412 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7 ± 0.3	0.303 ± 0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.