INTEGRATED CIRCUITS

MHTL

*MC660 P,L Series (−30°C to +75°C)
*MC660TL Series (−55°C to +125°C)

Motorola's MHTL integrated circuits are especially designed to meet the requirements of industrial applications because of the outstanding noise immunity. MHTL circuits provide error-free operation in high noise environments far beyond the tolerance of other integrated circuit families. Multifunction packages and broad operating temperature range further tailor this device family to the industrial designer's requirements.

*MHTL cermaic dual in-line devices are available with specification over the -55°C to +125°C temperature range and/or with hi-rel processing on special order. See your Motorola representative for pricing.

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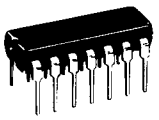
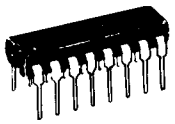
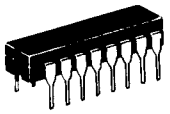


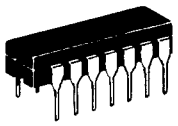
P SUFFIX
PLASTIC PACKAGE
CASE 646



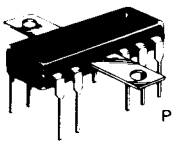
P SUFFIX
PLASTIC PACKAGE
CASE 648



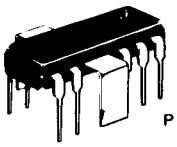
TL, L SUFFIX
CERAMIC PACKAGE
CASE 620



TL, L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 675



PC SUFFIX
PLASTIC PACKAGE
CASE 676

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 15 V ± 1.0 Vdc, T_A = 25°C)

Function	Type	Loading Factor Each Output	Propagation Delay ns typ	Power Dissipation mW typ/pkg	Case
Expandable Dual 4-Input NAND Gate (active pullup)	MC660	10	110	88/26 ②	632,646
Expandable Dual 4-Input NAND Gate (passive pullup)	MC661	10	125	88/26 ②	632,646
Expandable Dual 4-Input Line Driver (NAND)	MC662	30	140	180/26 ②	632,646
Dual J-K Flip-Flop	MC663	9	3.0 MHz ③	200	632,646
Master-Slave R-S Flip-Flop	MC664	8	3.0 MHz ③	160	632,646
Triple Level Translator	MC665	MDTL = 8 MTTL III = 5.5 MRTL = 5	40	83 (MDTL) 104 (MRTL)	632,646
Triple Level Translator	MC666	10	75	105	632,646
Dual Monostable Multivibrator	MC667	10	140	240	632,646
Quad 2-Input NAND Gate (passive pullup)	MC668	10	125	176/52 ②	632,646
Dual 4-Input Expander	MC669	–	–	–	632,646
Triple 3-Input NAND Gate (passive pullup)	MC670	10	125	132/39 ②	632,646
Triple 3-Input NAND Gate (active pullup)	MC671	10	110	132/39 ②	632,646
Quad 2-Input NAND Gate (active pullup)	MC672	10	110	176/52 ②	632,646
Dual 2-Input AND-OR-INVERT Gate (active pullup)	MC673	10	110	160/50 ②	632,646
Dual 2-Input AND-OR-INVERT Gate (passive pullup)	MC674	10	125	160/50 ②	632,646
Dual Pulse Stretcher/Multivibrator	MC675	10	150 (pins 1,6) 110 (pins 5,6)	180	632,646
BCD-To-Decimal Decoder-Driver	MC676	–	500	380	620,648
Hex Inverter With Strobe (active pullup)	MC677	10	110	246/96 ②	620,648
Hex Inverter With Strobe (without output resistors)	MC678	10	125	192/96 ②	620,648
Dual Lamp/Line Driver	MC679,B	125	0.5 μs typ	250/30 ②	632,646
Hex Inverter (active pullup)	MC680	10	110	246/96 ②	632,646
Hex Inverter (open collector)	MC681	10	125	192/96 ②	632,646
Quad Latch	MC682	10	250	375	620,648
Quad 2-Input Exclusive OR Gate	MC683	10	–	380	632,646
Decade Counter	MC684	10	0.5 MHz ③	480	620,648
Binary Counter	MC685	10	0.5 MHz ③	480	620,648
4-Bit Shift Register	MC686	10	0.5 MHz ③	480	620,648
Dual J-K Flip-Flop	MC688	10	2.5 MHz ③	375	620,648
Hex Inverter (high voltage)	MC689	10	150	173/55 ②	632,646
Hex Inverter (active pullup)	MC690	10	150	173/55 ②	632,646
Hex Inverter/Interface Element	MC691	10	300	500/150 ②	632,646
250 mA Quad 2-Input NAND Gate (Schmitt Trigger)	MC693	200	400	300	620,648
Dual Interface Element, Line Driver/Receiver (Schmitt Trigger)	MC696	10 @ 10 V V_{CC} 15 @ 25 V V_{CC}	400	225/60 ②	620,648
Hex Inverter (Passive Pull-up)	MC697	10	125	246/96 ②	632,646
500 mA Dual 2-Input AND Gate (Schmitt Trigger)	MC699	400	400	450	675,676

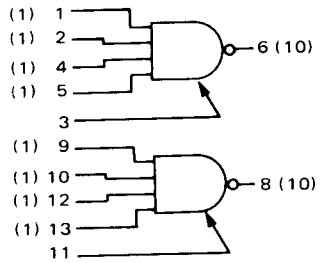
① L suffix denotes Dual In-Line Ceramic Package, P denotes Dual In-Line Plastic Package (i.e., MC660L = Dual In-Line Ceramic, MC660P = Dual In-Line Plastic Package)

② Logic High/Input Low ③ f_{Tog}

MHTL LOGIC DIAGRAMS

GATES

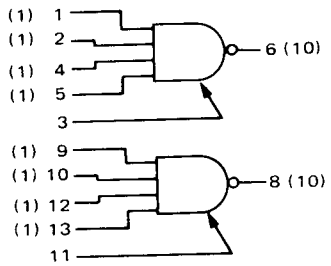
MC660
Expandable Dual 4-Input NAND Gate
(active output pullup)



$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$

t_{pd} = 110 ns typ
P_D = 88 mW typ/pkg (Inputs High)
26 mW typ/pkg (Input Low)

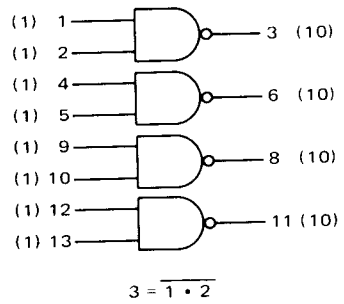
MC661
Expandable Dual 4-Input NAND Gate
(passive output pullup)



$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$

t_{pd} = 125 ns typ
P_D = 88 mW typ/pkg (Inputs High)
26 mW typ/pkg (Input Low)

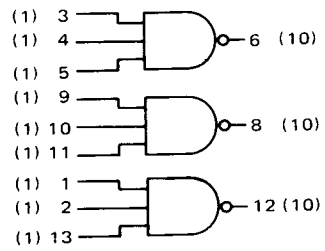
MC668
Quad 2-Input NAND Gate
(passive output pullup)



$3 = \overline{1 \cdot 2}$

t_{pd} = 125 ns typ
P_D = 176 mW typ/pkg (Inputs High)
52 mW typ/pkg (Input Low)

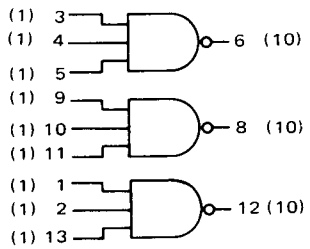
MC670
Triple 3-Input NAND Gate
(passive output pullup)



$6 = \overline{3 \cdot 4 \cdot 5}$

t_{pd} = 125 ns typ
P_D = 132 mW typ/pkg (Inputs High)
39 mW typ/pkg (Input Low)

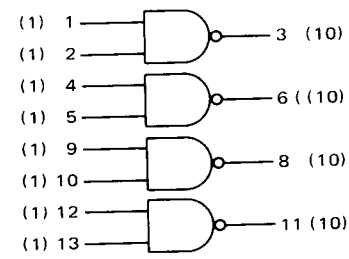
MC671
Triple 3-Input NAND Gate
(active output pullup)



$6 = \overline{3 \cdot 4 \cdot 5}$

t_{pd} = 110 ns typ
P_D = 132 mW typ/pkg (Inputs High)
39 mW typ/pkg (Input Low)

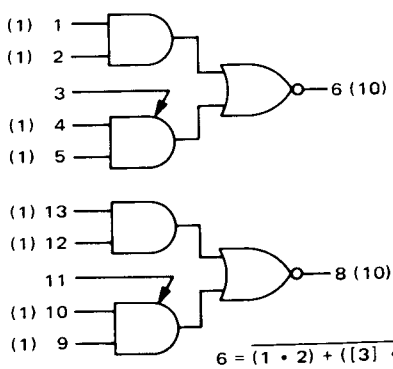
MC672
Quad 2-Input NAND Gate
(active output pullup)



$3 = \overline{1 \cdot 2}$

t_{pd} = 110 ns typ
P_D = 176 mW typ/pkg (Inputs High)
52 mW typ/pkg (Input Low)

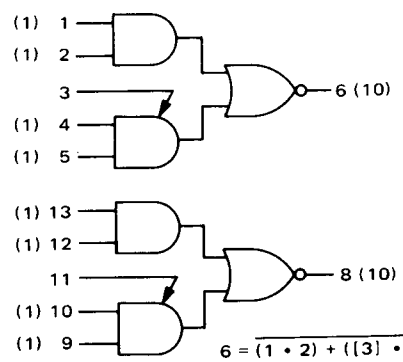
MC673
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate
(active output pullup)



$6 = \overline{(1 \cdot 2) + ([3] \cdot 4 \cdot 5)}$

t_{pd} = 110 ns typ
P_D = 160 mW typ/pkg (Inputs High)
50 mW typ/pkg (Input Low)

MC674
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate
(passive output pullup)



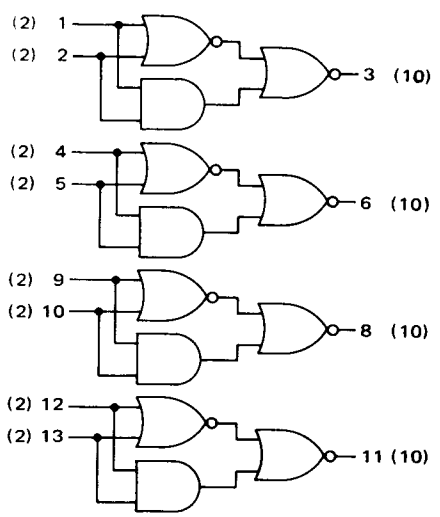
$6 = \overline{(1 \cdot 2) + ([3] \cdot 4 \cdot 5)}$

t_{pd} = 125 ns typ
P_D = 160 mW typ/pkg (Inputs High)
50 mW typ/pkg (Input Low)

Numbers at ends of terminals represent pin numbers.
Numbers in parenthesis indicate loading.
(V_{CC} = Pin 14, Gnd = Pin 7 for Case 646 and 632; V_{CC} = Pin 16, Gnd = Pin 8 for Case 648 and 620.)

GATES (continued)

MC683
Quad 2-Input Exclusive OR

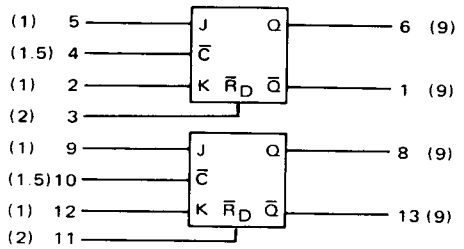


$3 = 1 \cdot \overline{2} + \overline{1} \cdot 2$

P_D = 380 mW typ/pkg

FLIP-FLOPS

MC663
Dual J-K Flip-Flop



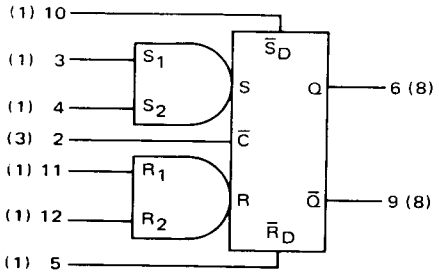
f_{Tog} = 3.0 MHz typ
P_D = 200 mW typ/pkg

TRUTH TABLE

t_n		t_{n+1}	
J	K	Q	$\overline{Q}$
0	0	Q_n	$\overline{Q}_n$
1	0	1	0
0	1	0	1
1	1	$\overline{Q}_n$	Q_n

Direct input ($\overline{R}_D$) must be high.
0 = low state
1 = high state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
O_n = state of Q output in time period t_n
NOTE: A low state "0" at the direct reset $\overline{R}_D$ causes a low state "0" at the Q output and the complement at the $\overline{Q}$ output.

MC664
Master-Slave R-S Flip-Flop



f_{Tog} = 3.0 MHz typ
P_D = 160 mW typ/pkg

DIRECT INPUT OPERATION

$\overline{R}_D$	$\overline{S}_D$	Q	$\overline{Q}$
1	1	NC	NC
1	0	1	0
0	1	0	1
0	0	NA	NA

Clock Input ($\overline{C}$) must be low
0 = low state
1 = high state
NC = No change
NA = Not allowed

CLOCKED OPERATION

t_n				t_{n+1}
S_1	S_2	R_1	R_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

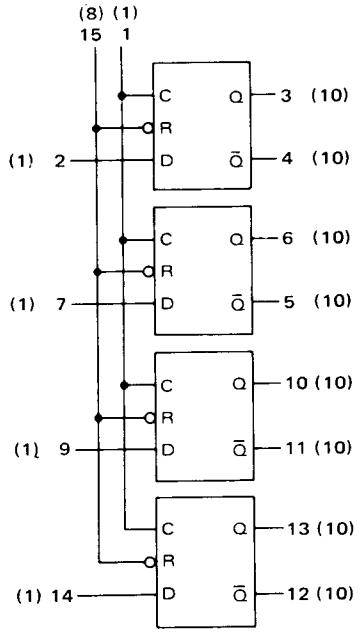
Direct inputs ($\overline{R}_D$, $\overline{S}_D$) must be high.

X = state of input does not affect state of the circuit
U = indeterminate state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

(continued)

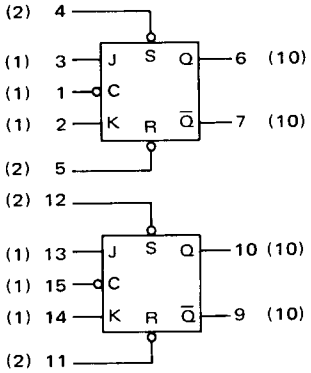
FLIP-FLOPS (continued)

MC682
Quad Latch



t_{pd} = 250 ns typ
P_D = 375 mW typ/pkg

MC688
Dual J-K Flip-Flop



TRUTH TABLE

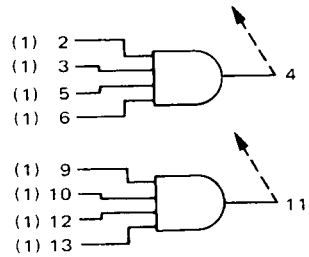
	R	S	t_n J	t_n K	t_{n+1} Q	t_{n+1} Q̄
•	0	1	x	x	0	1
•	1	0	x	x	1	0
	1	1	0	0	Q_n	$\bar{Q}_n$
	1	1	0	1	0	1
	1	1	1	0	1	0
	1	1	1	1	Q_n	$\bar{Q}_n$

0 = Low state
1 = High state
x = Don't care
t_n = Time period prior to negative transition of clock pulse.
t_{n+1} = Time period subsequent to negative transition of clock pulse.
Q_n = State of Q output in time period t_n.
• = Clock pulse must be in low state

f_{Tog} = 2.5 MHz typ
P_D = 375 mW typ/pkg

EXPANDER

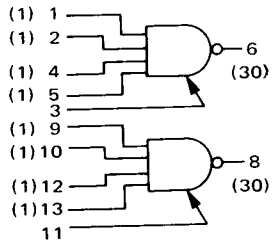
MC669
Dual 4-Input Expander



$4 = 2 \cdot 3 \cdot 5 \cdot 6$

DRIVERS

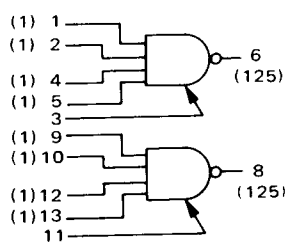
MC662
Expandable
Dual 4-Input Line Driver
(active output pullup)



$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$

t_{pd} = 140 ns typ
P_D = 180 mW typ/pkg (Inputs High)
26 mW typ/pkg (Input Low)

MC679, MC679B
Dual Lamp Driver

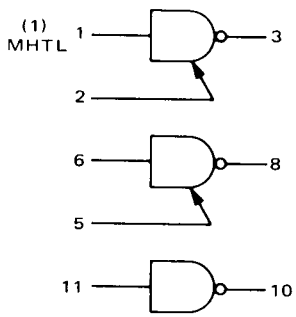


$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$

t_{pd} = 0.5 µs typ
P_D = 250 mW (Inputs High)
30 mW (Input Low)

TRANSLATORS

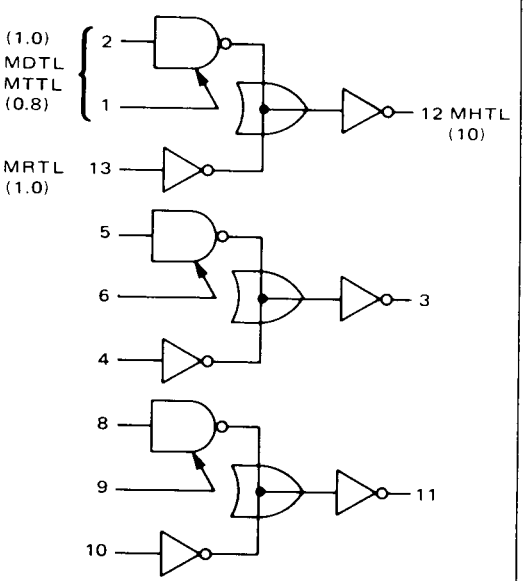
MC665
Triple Level Translator



$3 = \overline{1 \bullet [2]}$

t_{pd} = 40 ns typ
P_D = 83 mW typ/pkg (MDTL)
104 mW typ/pkg (MRTL)

MC666
Triple Level Translator

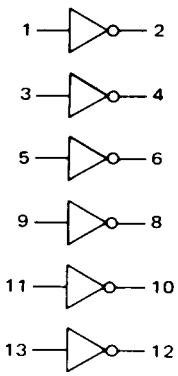


$12 = 2 \bullet [1] + 13$

t_{pd} = 75 ns typ
P_D = 105 mW typ/pkg

INVERTERS

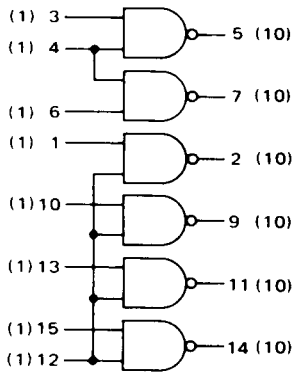
MC691
Hex Inverter/Translator
(low level to high level)



Positive Logic: $2 = \overline{1}$

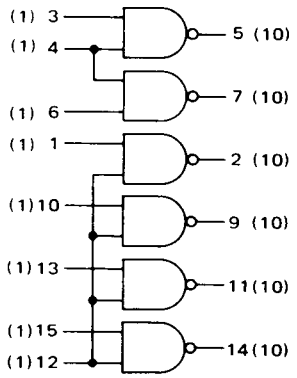
Input Loading Factor = 0.4
Output Loading Factor = 10
Propagation Delay Time:
t_{+-} = 150 ns typ
t_{-+} = 300 ns typ
Typical Total Power Dissipation:
Inputs High = 500 mW typ/pkg
Input Low = 150 mW typ/pkg

MC677
Hex Inverter With/Strobe
(active pullup)



t_{pd} = 110 ns typ
P_D = 246 mW typ/pkg (Inputs High)
96 mW typ/pkg (Input Low)

MC678
Hex Inverter With/Strobe
(without output resistors)



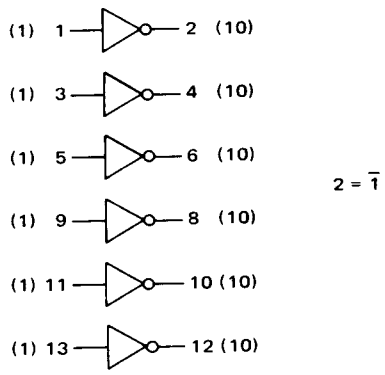
t_{pd} = 125 ns typ
P_D = 192 mW typ/pkg (Inputs High)
96 mW typ/pkg (Inputs Low)

(continued)

MHTL LOGIC DIAGRAMS

INVERTERS (continued)

MC680
Hex Inverter
(active pullup)

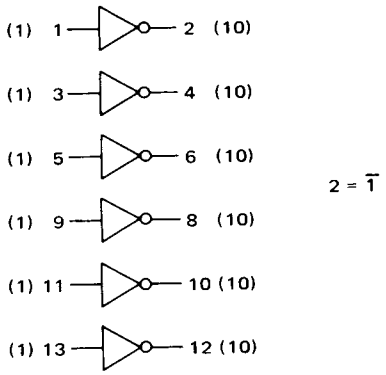


$2 = \overline{1}$

t_{pd} = 110 ns typ
P_D = 246 mW typ/pkg (Inputs High)
96 mW typ/pkg (Input Low)

MC681
Hex Inverter
(open collector)

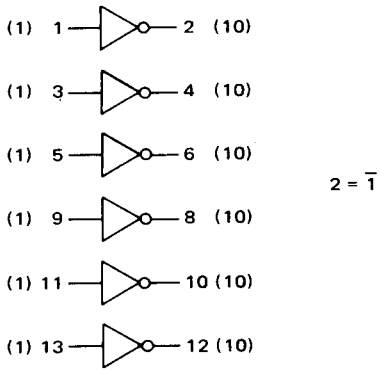
MC697
Hex Inverter
(passive pull-up)



$2 = \overline{1}$

t_{pd} = 125 ns typ
P_D = 192 mW typ/pkg (Inputs High)
96 mW typ/pkg (Input Low)

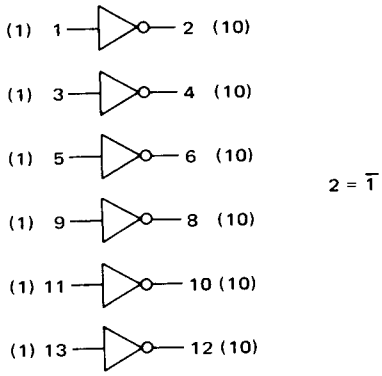
MC689
Hex Inverter
(high voltage)



$2 = \overline{1}$

t_{pd} = 150 ns typ
P_D = 173 mW typ/pkg (Inputs High)
55 mW typ/pkg (Inputs Low)

MC690
Hex Inverter
(active pullup)

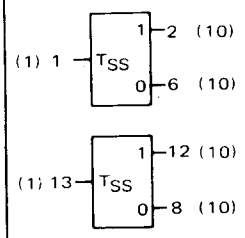


$2 = \overline{1}$

t_{pd} = 150 ns typ
P_D = 173 mW typ/pkg (Inputs High)
55 mW typ/pkg (Inputs Low)

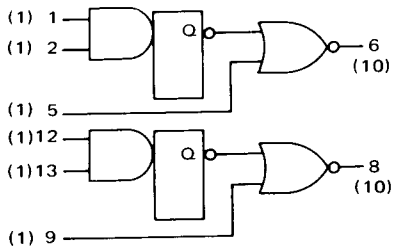
MULTIVIBRATORS

MC667
Dual Monostable Multivibrator



t_{pd} = 140 ns typ
P_D = 240 mW typ/pkg

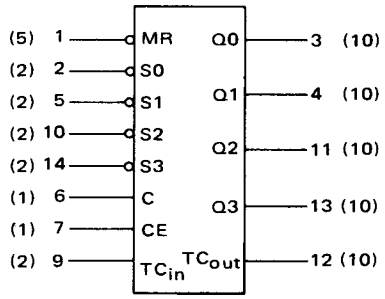
MC675
Dual Pulse Stretcher/Multivibrator



t_{pd} = 150 ns typ (Pins 1, 6)
110 ns typ (Pins 5, 6)
P_D = 180 mW typ/pkg

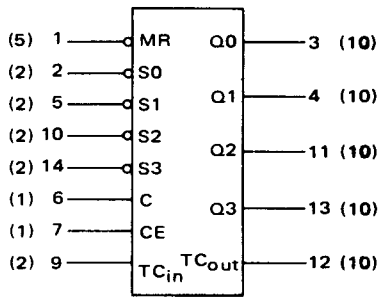
COUNTERS

MC684
Decade Counter



f_{Tog} = 0.5 MHz min
P_D = 480 mW typ/pkg

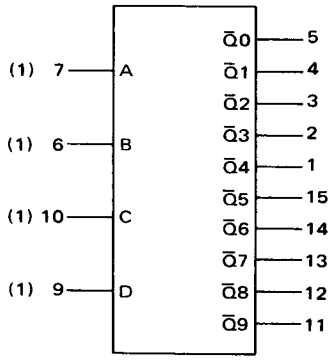
MC685
Binary Counter



f_{Tog} = 0.5 MHz min
P_D = 480 mW typ/pkg

DECODER

MC676
BCD-To-Decimal Decoder-Driver

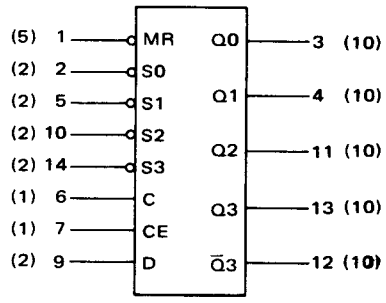


t_{pd} = 500 ns Typ

Power Dissipation = 380 mW typ/pkg

SHIFT REGISTER

MC686
4-Bit Shift Register



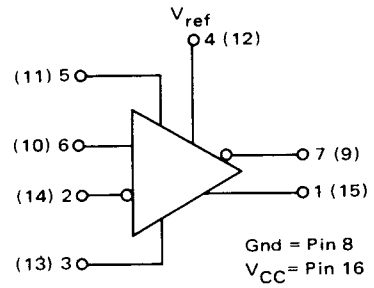
f_{Tog} = 0.5 MHz min
P_D = 480 mW typ/pkg

MHTL LOGIC DIAGRAMS

LINE DRIVER/RECEIVER

MC696
Dual Interface Element,
Line Driver/Receiver

(1/2 Device Shown)

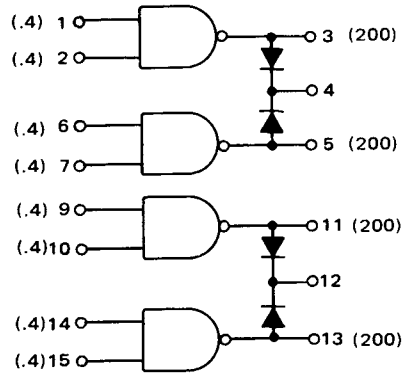


Numbers in parenthesis denotes pin numbers for other half of device.

t_{pd} = 400 ns typ
P_D = 225 mW typ/pkg (Inputs High)
96 mW typ/pkg (Inputs Low)

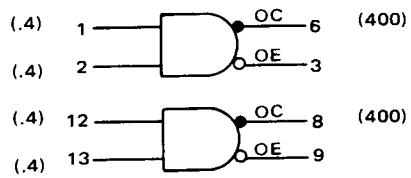
DRIVERS

MC693
250 mA Quad 2-Input NAND Driver
(open collector, high voltage output with inductive load clamp)
(Schmitt Trigger Inputs)



t_{pd} = 400 ns Typ
P_D = 300 mW Typ/Pkg.

MC699
500 mA Dual 2-Input AND Gate/Driver
(high voltage output)
(Schmitt Trigger Inputs)



OE = Open Emiter
OC = Open Collector

Positive Logic (with Pin 3 at Gnd): 6 = 1 • 2
Input Loading Factor = 0.415*
Propagation Delay Time - 360 ns typ*
Typical Total Power Dissipation = 450 mW typ/pkg*
*= V_{CC} = 15 V

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage Continuous Pulsed, 1.0 s	V_{CC}	 18 20	Vdc
Input Voltage MC666 MDTL MRTL All Others	V_{in}	 -1.0 to +6.0 -4.0 to +4.0 -1.0 to +18	Vdc
Output Current (into outputs) MC662 MC663 MC664 MC669 All Others except Power Drivers	–	 60 28 26 30	mAdc
Input Reverse Current @ 18 V	I_R	0.5	mAdc
Forward Current (individual) MC669P	I_F	30	mAdc
Operating Temperature Range	T_A	-30 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C