

# Z86K13/K14/K15 K16/K17/K18

CMOS Z8<sup>®</sup> 8-BIT MCU  
KEYBOARD CONTROLLERS

## FEATURES

Device	ROM (KB)	I/O Lines	Speed (MHz)	Pin Count/Package
Z86K13	2	32	4-5	40-DIP, 44-PLCC, 44-QFP, COB
Z86K14	3	32	4-5	40-DIP, 44-PLCC, 44-QFP, COB
Z86K15	4	32	4-5	40-DIP, 44-PLCC, 44-QFP, COB
Z86K16	2	32	4-5	40-DIP, 44-PLCC, 44-QFP, COB
Z86K17	3	32	4-5	40-DIP, 44-PLCC, 44-QFP, COB
Z86K18	4	32	4-5	40-DIP, 44-PLCC, 44-QFP, COB

- 4.5V to 5.5 V Operating Range
- 0°C to +70°C Operating Temperature Range
- 188 Bytes of Ram

- Low-Power Consumption: 60 mW @ 5 MHz
- Five Vectored, Priority Interrupts from Five Different Sources
- A Programmable 8-Bit Counter/Timer, with 6-Bit Programmable Prescaler
- Power-On-Reset (POR) Timer, Hardware Watch-Dog Timer (WDT)
- Digital Inputs CMOS Levels with Internal Pull-Up Resistors
- Four Direct Connect LED Drive Ports
- On-Chip RC Oscillator (Z86K13/14/15)
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive (Z86K16/17/18)
- Low System EMI Emission

## GENERAL DESCRIPTION

The Z86KXX Keyboard Controllers are full-featured members of the Z8<sup>®</sup> MCU family offering a unique register-to-register architecture that avoids accumulator bottlenecks and is more code efficient than RISC processors.

For keyboard applications demanding powerful I/O capabilities, the Z86KXX provides 32 pins dedicated to input and output for row, column, clock, data, and LEDs.

The on-chip counter/timer is available to relieve the system of administering real-time tasks.

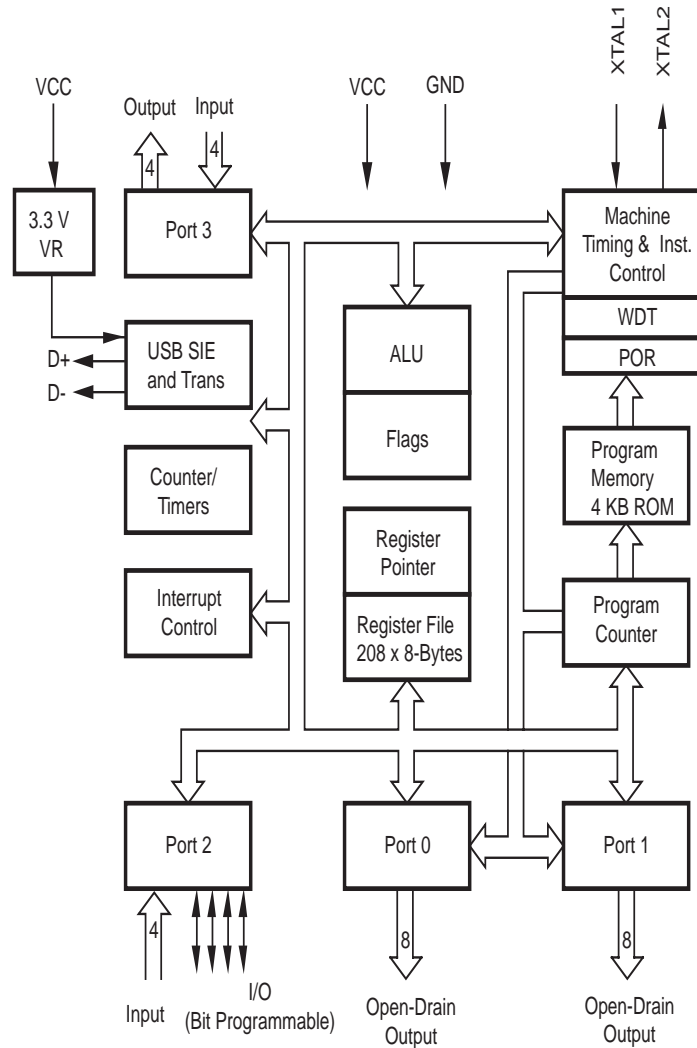
Five different internal or external interrupt sources are maskable and prioritized in which a vectored address is provided for efficient interrupt subroutine handling and multitasking functions.

The Z86K15 achieves low EMI by means of several modifications in the output drivers and clock circuitry of the device.

**GENERAL DESCRIPTION** (Continued)

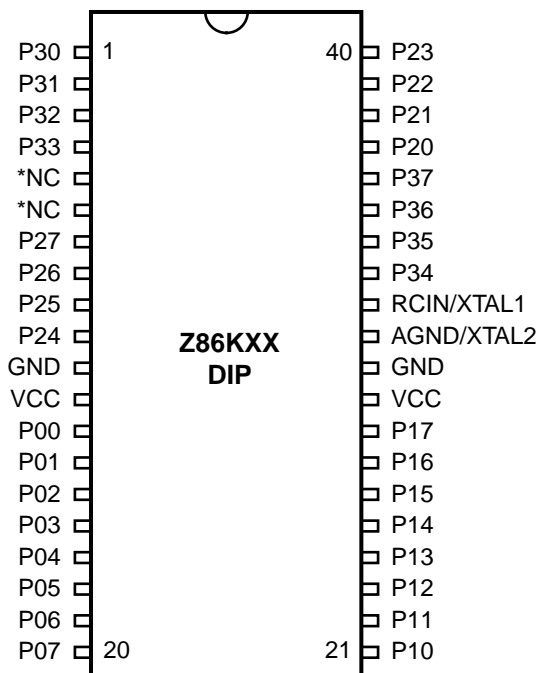
**Notes:** All signals with a preceding front slash, “/”, are active Low. For example, B/W (WORD is active Low); /B/W (BYTE is active Low, only). Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V <sub>CC</sub>	V <sub>DD</sub>
Ground	GND	V <sub>SS</sub>



**Figure 1. Z86KXX Functional Block Diagram**

## PIN DESCRIPTION

**Notes:**

\*Pin 5 and 6 used for testing Ground during normal operation.

When Pin 5 is connected to  $V_{cc}$ . Pin 6 is CLK OUT.

When Pin 5 is connected to GND, Pin 6 outputs nothing.

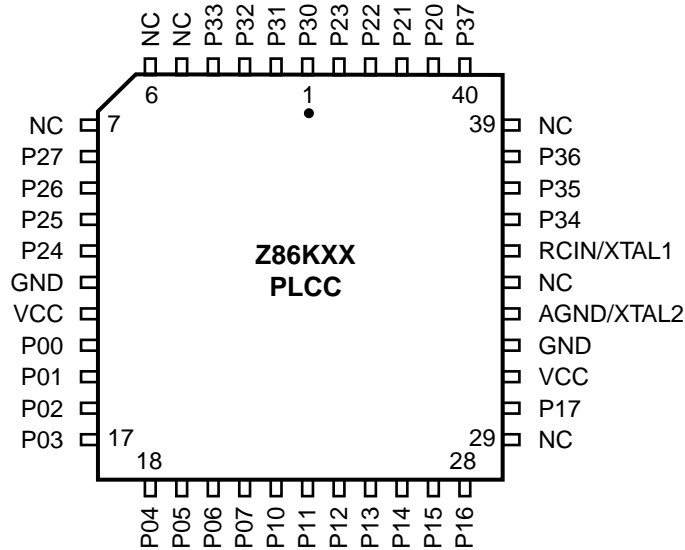
These pins must be tied to ground in application.

**Figure 2. 40-Pin DIP Configuration**

**Table 1. 40-Pin DIP Pin Identification**

Pin #	Symbol	Function	Direction
1-4	P30-P33	Port 3, Pins 0,1,2,3	Input
5-6	NC	Tied to GND	
7-10	P27-P24	Port 2, Pins 7,6,5,4	In/Output
11	GND	Ground	
12	$V_{cc}$	Power Supply	Input
13-20	P00-P07	Port 0, Pins 0,1,2,3,4,5,6,7	Output
21-28	P10-P17	Port 1, Pins 0,1,2,3,4,5,6,7	Output
29	$V_{cc}$	Power Supply	
30	GND	Ground	
31	AGND/XTAL2	Analog Ground or Crystal Clock Out	
32	RCIN/XTAL1	RCIN/Crystal Oscillator Clock	Input
33-36	P34-P37	Port 3, Pins 4,5,6,7	Output
37-40	P20-P23	Port 2, Pins 0,1,2,3	Input

**PIN DESCRIPTION** (Continued)



**Notes:**

Pins 5 and 6 used for testing. Ground during normal operation  
When Pin 43 is connected to V<sub>cc</sub>, Pin 44 is CLKOUT.  
When Pin 43 is connected to GND. Pin 44 outputs nothing.

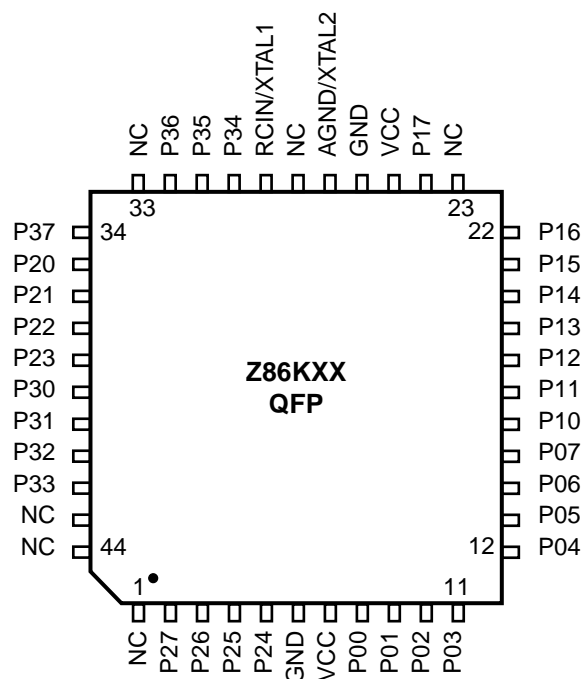
**Figure 3. 44-Pin PLCC Pin Assignments**

**Table 2. 44-Pin PLCC Pin Assignments**

Pin #	Symbol	Function	Direction
1-4	P30-P33	Port 3, Pins 0,1,2,3	Input
5-7	NC	Test Pins (GND)	
8-11	P27-P24	Port 2, Pins 4,5,6,7	In/Output
12	GND	Ground	
13	V <sub>cc</sub>	Power Supply	
14-21	P00-P07	Port 0, Pins 0,1,2,3,4,5,6,7	Output
22-28	P10-P16	Port 1, Pins 0,1,2,3,4,5,6	Output
29	NC	Not Connected	

**Table 2. 44-Pin PLCC Pin Assignments**

Pin #	Symbol	Function	Direction
30	P17	Port 1, Pin 7	Output
31	V <sub>cc</sub>	Power Supply	
32	GND	Ground	
33	AGND/ XTAL2	Analog Ground or Crystal Clock Out	
34	NC	Not Connected	
35	RCIN/ XTAL1	RCIN/Crystal Oscillator Clock	Input
36-38	P34-P37	Port 3, Pins 4,5,6,7	Output
39	NC	Not Connected	
40	P37	Port 3, Pin 7	Output
41-44	P20-P23	Port 2, Pins 0,1,2,3	In/Output

**Notes:**

Pins 43 and 44 are used for testing ground during normal operation.  
 When Pin 45 is connected to  $V_{cc}$ , Pin 46 is CLKOUT.  
 When Pin 45 is connected to GND. Pin 46 outputs nothing.

**Figure 4. 44-Pin QFP Pin Assignments****Table 3. 44-Pin QFP Pin Identification**

Pin #	Symbol	Function	Direction
1	NC	Not Connected	
2-5	P24-P27	Port 2, Pins 4,5,6,7	In/Output
6	GND	Ground	
7	$V_{cc}$	Supply Voltage	
8-15	P00-P07	Port 0, Pins 0,1,2,3,4,5,6,7,	Output
16-22	P10-P16	Port 1, Pins 0,1,2,3,4,5,6	Output
23	NC	Not Connected	
24	P17	Port 1, Pin 7	Output
25	$V_{cc}$	Supply Voltage	

**Table 3. 44-Pin QFP Pin Identification**

Pin #	Symbol	Function	Direction
26	GND	Ground	
27	AGND/ XTAL2	Analog Ground/ Crystal Clock Out	
28	NC	Not Connected	
29	RCIN / XTAL1	RCIN/Crystal Oscillator Clock	Input
30-32	P34-P36	Port 3, Pins 4,5,6	Output
33	NC	Not Connected	
34	P37	Port 3, Pin 7	Output
35-38	P20-P23	Port 2, Pins 0,1,2,3	Input
39-42	P30-P33	Port 3, Pins 0,1,2,3	Input
43-44	NC	Test Pins (GND)	

## ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
$V_{CC}$	Supply Voltage*	-0.3	+7.0	V
$T_{STG}$	Storage Temp	-65	+150	°C
$T_A$	Oper Ambient Temp	0	+105	°C

**Note:** \* Voltage on all pins with respect to GND.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## STANDARD TEST CONDITIONS

The characteristics listed here apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 5).

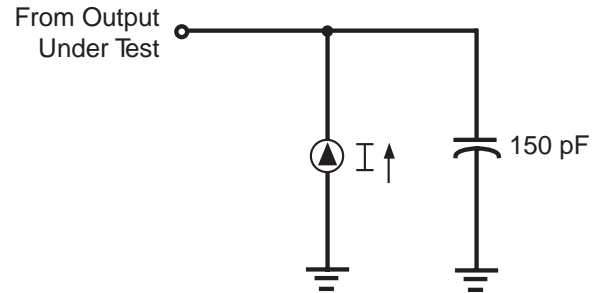


Figure 5. Test Load Diagram

## CAPACITANCE

$T_A = 25^\circ\text{C}$ ;  $V_{CC} = \text{GND} = 0\text{V}$ ;  $f = 1.0 \text{ MHz}$ ; unmeasured pins returned to GND.

Parameter	Max
Input Capacitance	12 pF
Output Capacitance	12 pF
I/O Capacitance	12 pF

Frequency tolerance  $\pm 10\%$

**DC CHARACTERISTICS**

$$V_{CC} = 5.0V \pm 10\% @ 0^{\circ}C \text{ to } +70^{\circ}C$$

Sym	Parameter	Min	Max	Typ*	Unit	Condition
$V_{CH}$	Clock Input High Voltage	$0.7 V_{CC}$	$V_{CC} + 0.3V$	2.5	V	Driven by External Clock Generator
$V_{CL}$	Clock Input Low Voltage	GND -0.3	$0.2 V_{CC}$	1.5	V	Driven by External Clock Generator
$V_{IH}$	Input High Voltage	$0.7 V_{CC}$	$V_{CC} + 0.3$	2.5	V	
$V_{IL}$	Input Low Voltage	GND -0.3	$0.2 V_{CC}$	1.5	V	
$V_{OH}$	Output High Voltage	$V_{CC} - 0.4$		4.7	V	$I_{OH} = -2.0 \text{ mA}$
$V_{OH}$	Output High Voltage	$V_{CC} - 0.6$			V	$I_{OH} = -2.0 \text{ mA}$ (see note 1 below.)
$V_{OL}$	Output Low Voltage		.4		V	$I_{OL} = 4 \text{ mA}$
$V_{OL}$	Output Low Voltage		.8		V	$I_{OL} = 4 \text{ mA}$ (see note 1 below.)
$I_{OL}$	Output Low	10	20		mA	$V_{OL} = V_{CC} - 2.2 \text{ V}$ (see note 1, 2 below.)
$I_{OL}$	Output Leakage	-1	1	<1	$\mu\text{A}$	$V_{IN} = 0V, 5.25V$
$I_{CC}$	$V_{CC}$ Supply Current		12	6	mA	@ 5.0 MHz
$I_{CC1}$	Halt Mode Current			2	mA	@ 5.0 MHz
$I_{CC2}$	Stop Mode Current		10		$\mu\text{A}$	
$R_p$	Pull Up Resistor	6.76	14.04	10.4	K ohm	
$R_p$	Pull Up Resistor (P26-P27)	1.8	3	2.4	K ohm	

**Notes:**

\* Typical @ 25°C

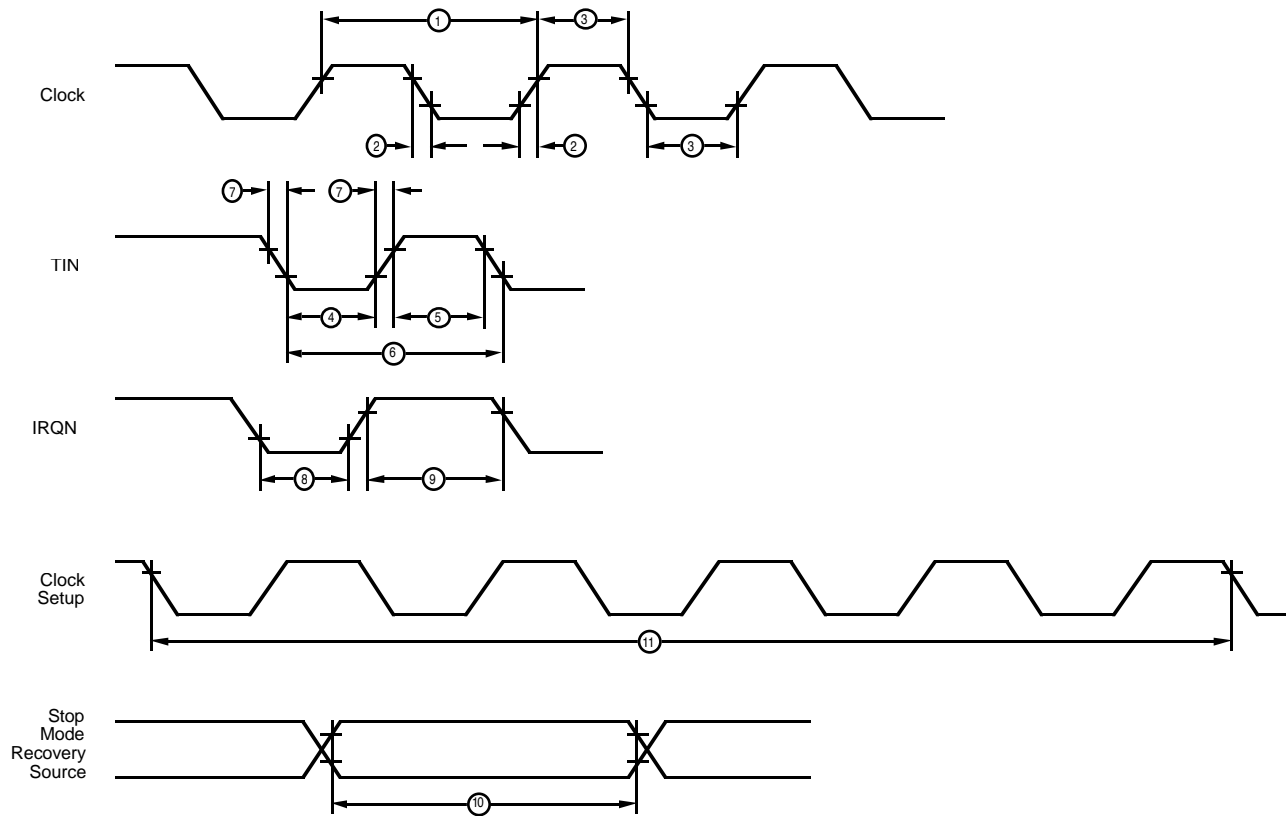
1. Ports P37-P34. These may be used for LEDs or as general-purpose outputs requiring high sink current.
2.  $V_{CC} = 5.0V \pm 5\% @ 0^{\circ}C \text{ to } +70^{\circ}C$

**AC ELECTRICAL CHARACTERISTICS**

No	Symbol	Parameter	V <sub>CC</sub> Note[4]	T <sub>A</sub> = 0°C to 70°C		Units	Notes
				5 MHz			
				Min	Max		
1	TpC	Input Clock Period	5.0V	200	250	ns	1
2	TrC,TfC	Clock Input Rise & Fall Times	5.0V		25	ns	1
3	TwC	Input Clock Width	5.0V	37		ns	1
4	TwTinL	Timer Input Low Width	5.0V	70		ns	1
5	TwTinH	Timer Input High Width	5.0V	2.5TpC			1
6	TpTin	Timer Input Period	5.0V	4TpC			1
7	TrTin,	Timer Input Rise & Fall Timer	5.0V		100	ns	
8A	TwlL	Int. Request Low Time	5.0V	70		ns	1,2
8B	TwlL	Int. Request Low Time	5.0V	3TpC			1,3
9	TwlH	Int. Request Input High Time	5.0V	3TpC			1,2
10	Twsm	STOP Mode Recovery Width Spec	5.0V	5TpC		ns	
11	Tost	Oscillator Start-up Time	5.0V		5TpC		
12	Twdt	Watch-Dog Timer Delay Time	5.0V	53		ms	
13	T <sub>POR</sub>	Power--On Reset	5.0V	106	130	ms	

**Notes:**

1. Timing Reference uses 0.7 V<sub>CC</sub> for a logic 1 and 0.2 V<sub>CC</sub> for a logic 0.
2. Interrupt request through Port 3 (P31-P33).
3. Interrupt request through Port 3 (P30).



**Figure 6. Additional Timing**



## PIN FUNCTIONS

**RCIN.** A precision resistor is connected between this pin and the power supply to form the precision RC oscillator.

**CLKOUT.** This pin is the system clock of the Z8® and runs at the frequency of the RC oscillator (Test only).

**Port 0** (P07-P00). Port 0 is an 8-bit, CMOS-compatible open-drain output (Figure 7).

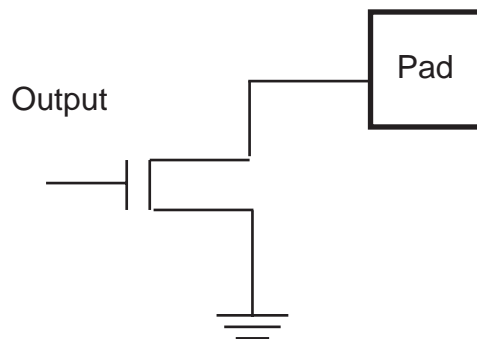
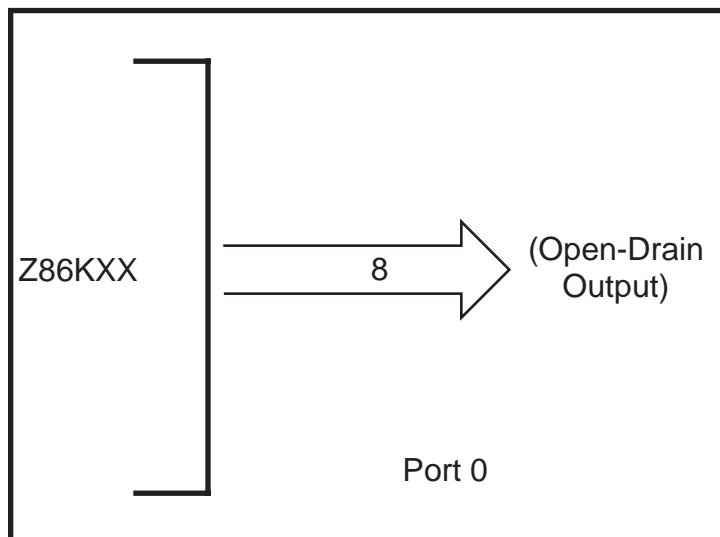
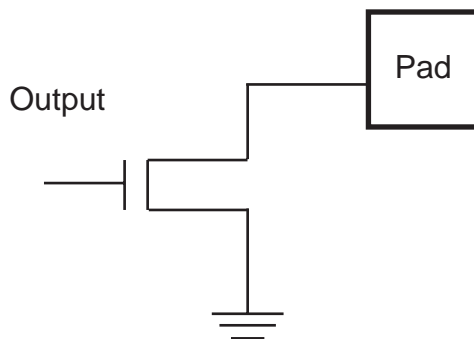
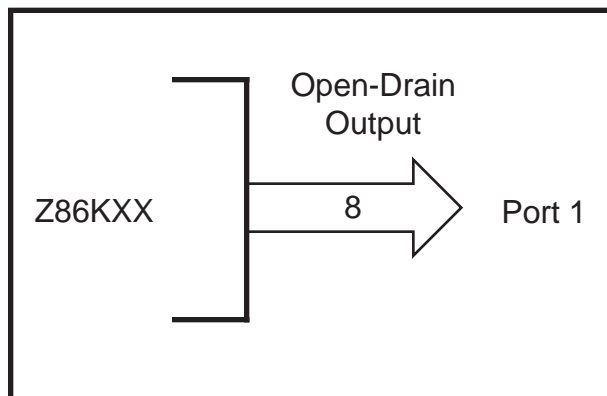


Figure 7. Port 0 Configuration

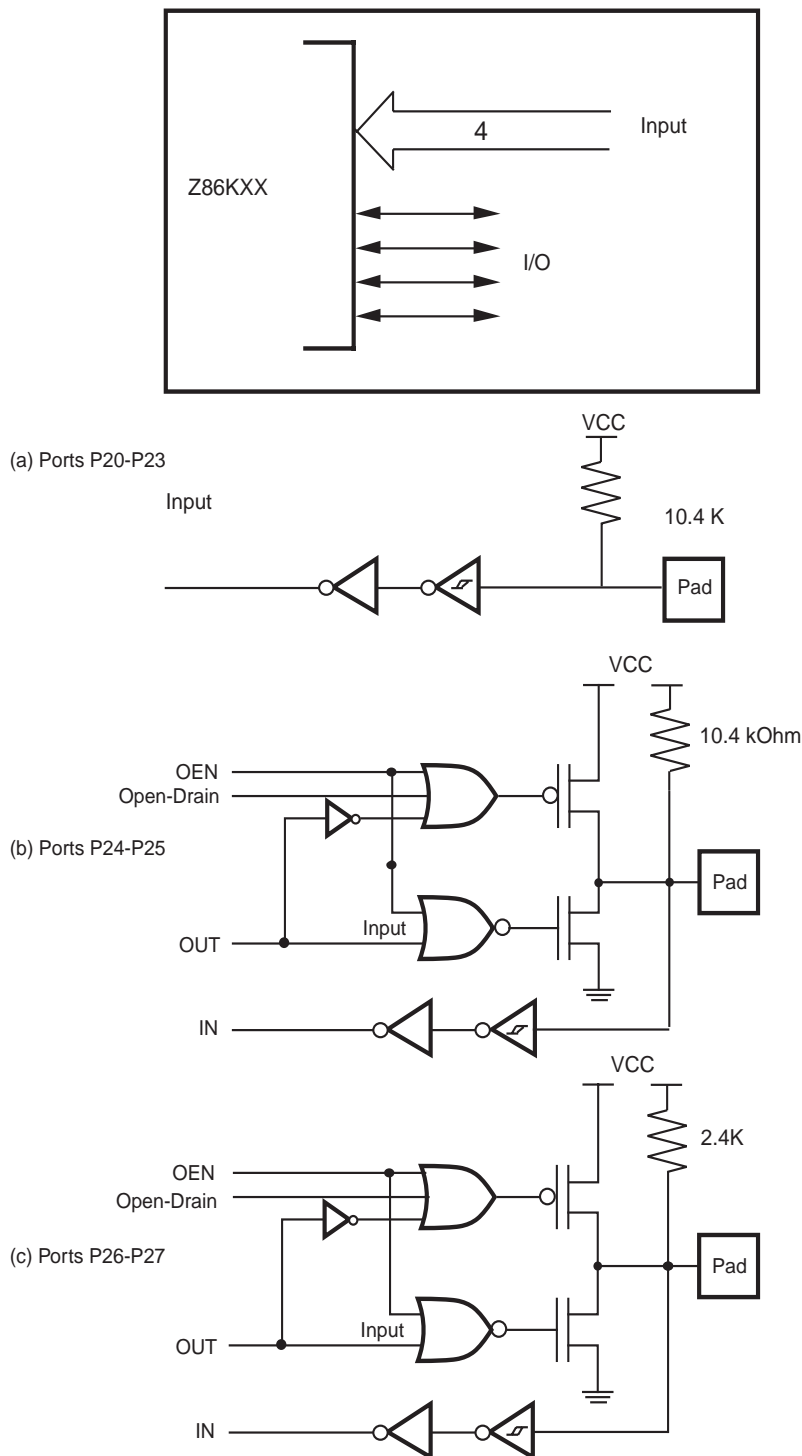
**Port 1** (P17-P10). Port 1 is an 8-bit CMOS compatible open-drain output port (Figure 8).



**Figure 8. Port 1 Configuration**

**Port 2** (P27-P20). Port 2 is an 8-bit CMOS compatible Port with 4-bit input, 4-bit programmable I/O (Figure 9). P20-

P25 have 10.4K ( $\pm 35\%$ ) pull-up resistors. P26-P27 have 2.4K ( $\pm 25\%$ ) pull-up resistors.

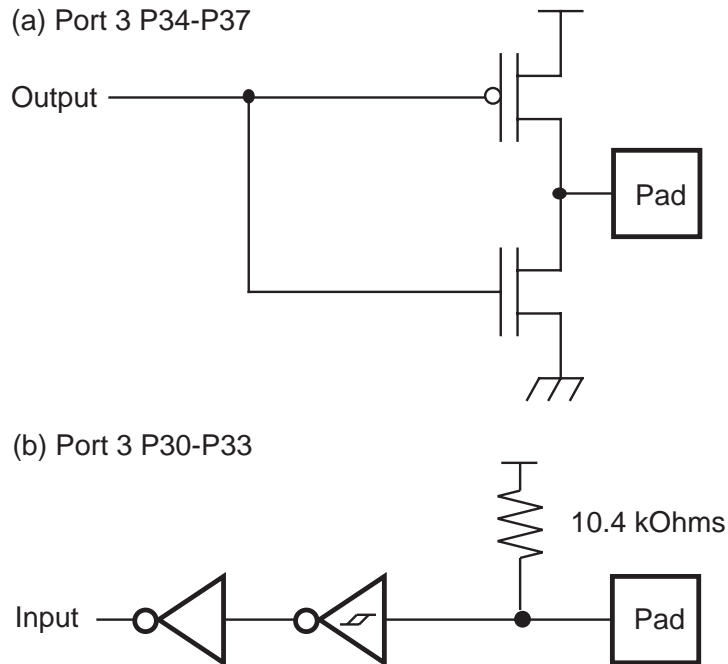
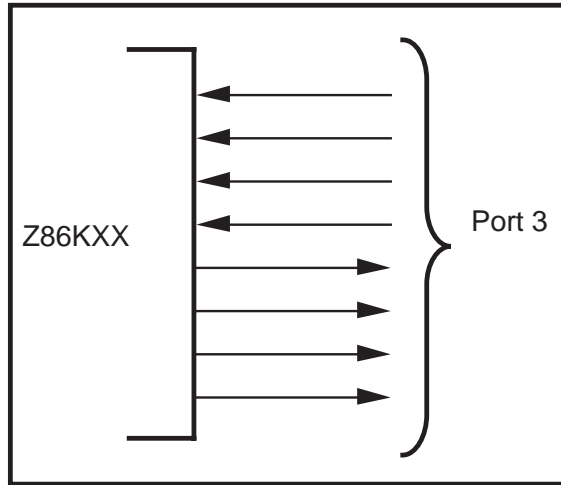


**Figure 9. Port 2 Configuration**

**PIN FUNCTIONS** (Continued)

**Port 3** (P37-P30). Port 3 is an 8-bit, CMOS-compatible four-fixed input (P33-P30) and four-fixed output (P37-P34) I/O port. Port 3 inputs have 10.4 Kohm pull-up resistors. Outputs are capable of directly driving LED.

Port 3 is configured under software control to provide four external interrupt request signals (IRQ0-IRQ3).



**Figure 10. Port 3 Configuration**

**Program Memory.** The 16-bit program counter addresses 4 KB of program memory space at internal locations (Figure 11).

The first 12 bytes of program memory are reserved for the interrupt vectors. These locations have six 16-bit vectors that correspond to the five available interrupts.

Byte 12 to byte 4095\* consists of on-chip, mask programmed ROM. Addresses 4096\* and greater are reserved. (\*2048 for K13/K16, 3072 for K14/K17)

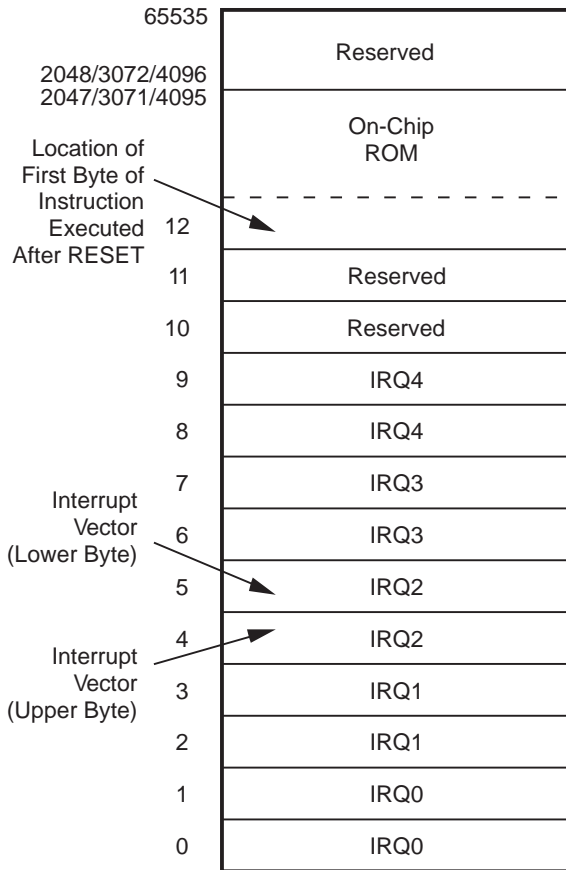


Figure 11. Program Memory Map

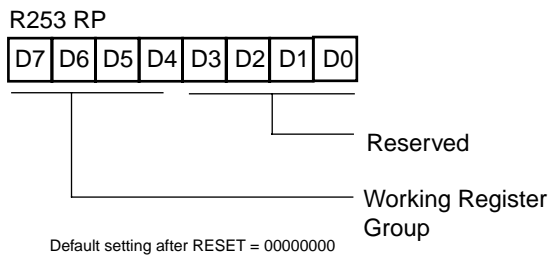


Figure 12. Register Pointer Register

**Register File.** The register file (Figure 13) consists of four I/O port registers, 188 general-purpose registers (excluding P00-P03), and 11 control and status registers (R3-R0, R191-R4, and R255-R240, respectively). The instructions can access registers directly or indirectly through an 8-bit address field. This allows short, 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into nine working-register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

LOCATION	IDENTIFIERS	
R255	Stack Pointer (Bits 7-0)	SPL
R254	Reserved	
R253	Register Pointer	RP
R252	Program Control Flags	FLAGS
R251	Interrupt Mask Register	IMR
R250	Interrupt Request Register	IRQ
R249	Interrupt Priority Register	IPR
R248	Reserved	
R247	Port 3 Mode	P3M
R246	Port 2 Mode	P2M
R245	T0 Prescaler	PREQ
R244	Timer/Counter0	T0
R243	Reserved	
R242	Reserved	
R241	Timer Mode	TMR
R240	Reserved	
	Not Implemented	
R 191	General-Purpose Registers	
R4		
R3	Port 3	P3
R2	Port 2	P2
R1	Port 1	P1
R0	Port 0	P0

Note:\* Will not be reset with a STOP Mode Recovery.

Figure 13. Register File Configuration

PIN FUNCTIONS (Continued)

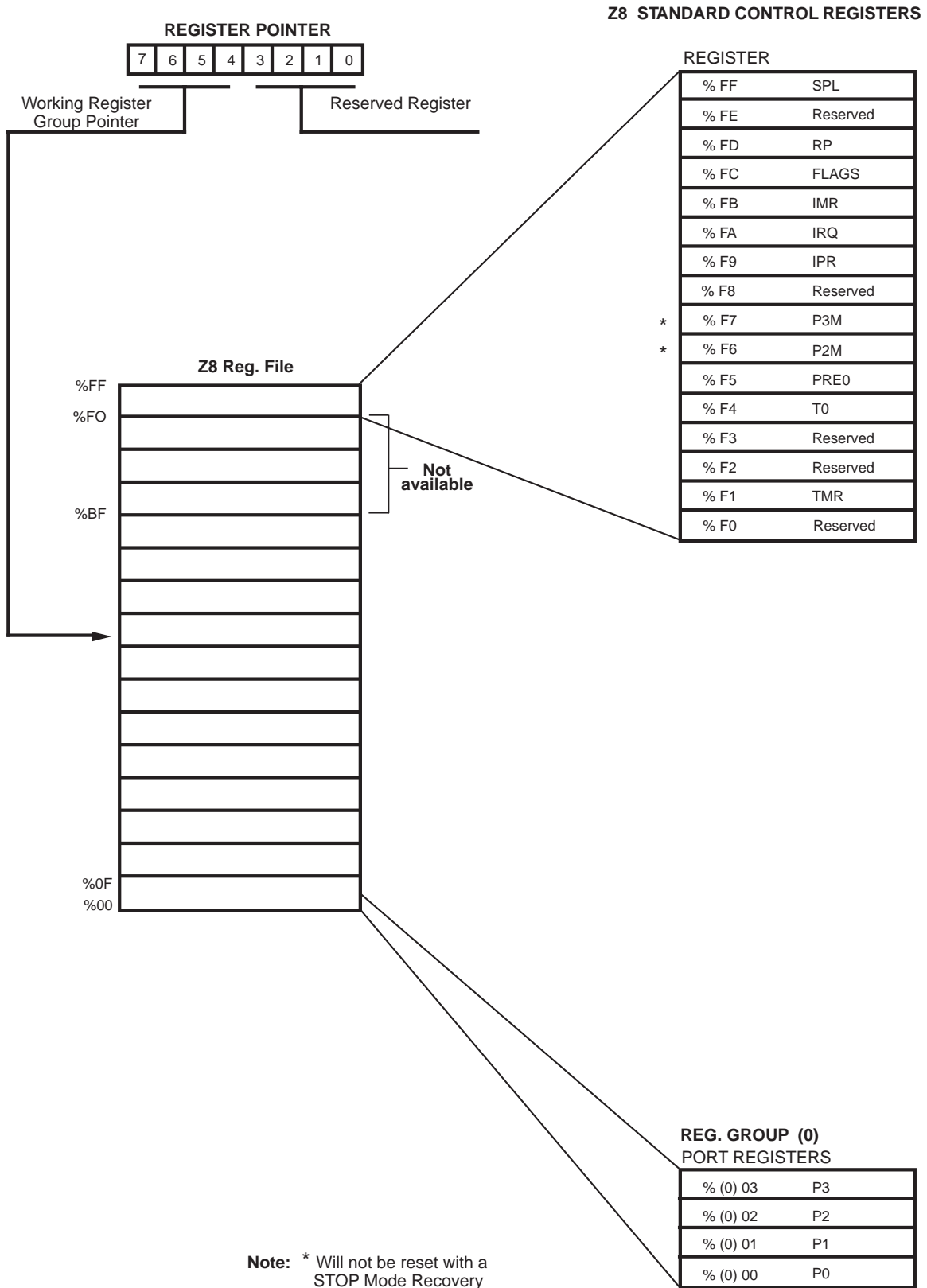


Figure 14. Register File Architecture

**Counter/Timers.** There is an 8-bit programmable counter/timer (T0) driven by its own 6-bit programmable prescaler (Figure 15).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. The prescaler drives its counter, which decrements the value (1 to 256) on the prescaler overflow. When both the counter and prescaler reach the end of count, a timer interrupt request, IRQ4, is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counter can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode) The counter, but not the prescaler, is read at any time without disturbing its value or count mode.

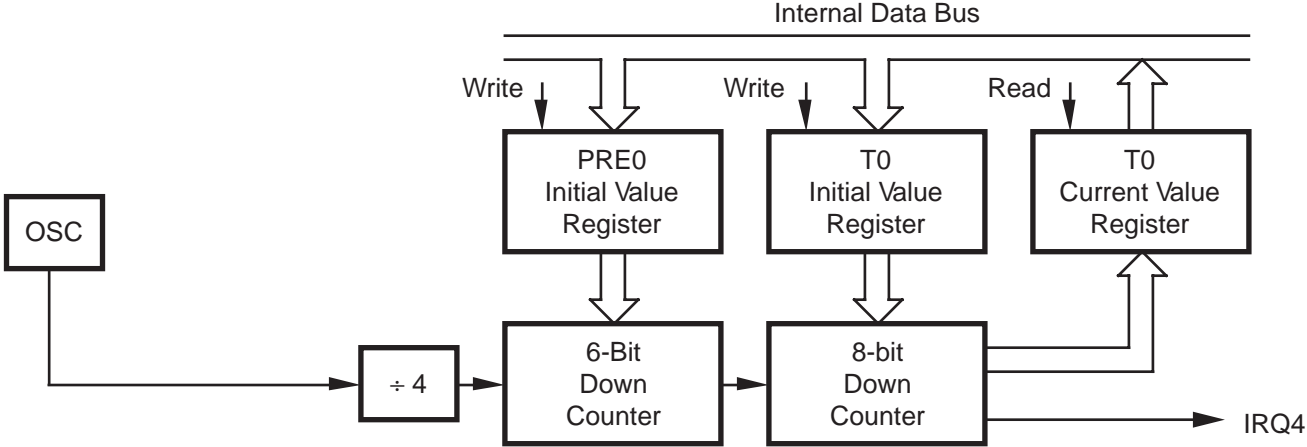


Figure 15. Counter/Timers Block Diagram

**PIN FUNCTIONS** (Continued)

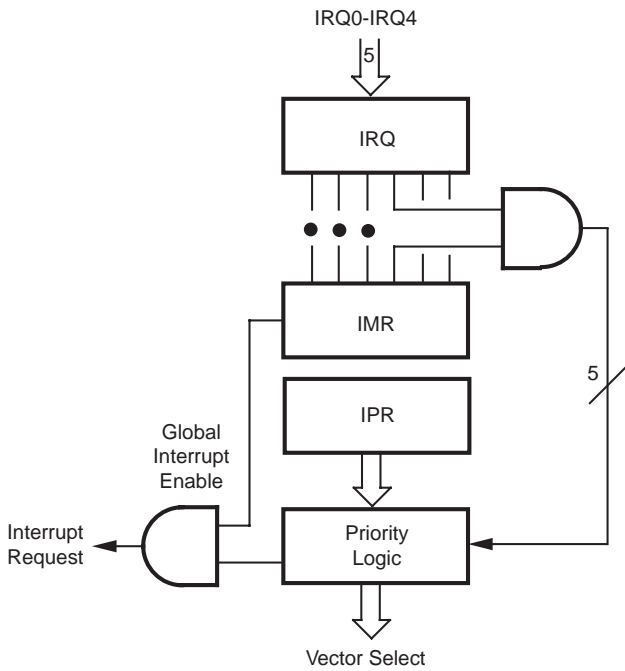
**Interrupts.** The Z86K15 has five different interrupts from five different sources. These interrupts are maskable and prioritized (Figure 16). The five sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, and the other is claimed by the counter/timer. The Interrupt Masked Register globally or individually enables or disables the five interrupts requests.

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated an interrupt request is granted. Thus, this disables all of the subsequent interrupts, saves the Program Counter and status flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

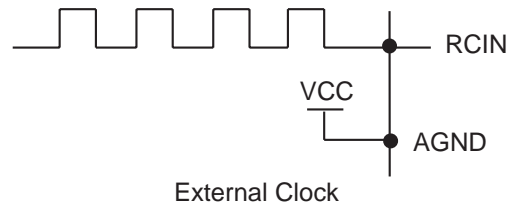
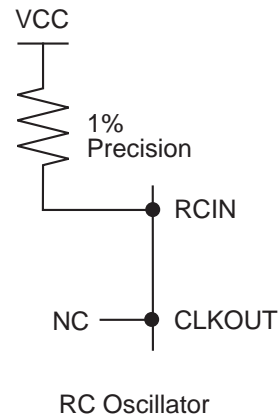
To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt request needs service.

**RC Oscillator.** The Z86K13/14/15 provides an internal capacitor to accommodate an RC oscillator configuration. A 1% precision resistor is necessary to achieve ±10% accurate frequency oscillation.

The Z86K15 also accepts external clock from (RCIN) with (AGND) connected to V<sub>CC</sub> (Figure 17).



**Figure 16. Interrupt Block Diagram**



**Figure 17. RC Oscillator Configuration**



**Watch-Dog Timer.** The Watch-Dog Timer is activated automatically by power-on if it is enabled in the Mask Option. The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is driven by the system clock. It must be refreshed at least once during each time cycle by executing the WDT instruction. WDT can be enabled by Mask Option. (Figure 18)

**WDT Hot bit.** Bit 7 of the Interrupt Request register (IRQ register FAH) determines whether a hot start or cold start occurred. A cold start is defined as reset occurring from

power-up of the Z86K15 (the default upon power-up is 0). A hot start occurs when a WDT time-out has occurred (bit 7 is set to 1). Bit 7 of the IRQ register is read-only and is automatically reset to 0 when read.

**Watch-Dog Timer .** The WDT time-out is  $\frac{294912\text{ms}}{f(\text{Hz})}$ .

**WDT During HALT (D5-R250).** This bit determines whether or not the WDT is active during HALT Mode. The default is 1, and a 1 indicates active during HALT.

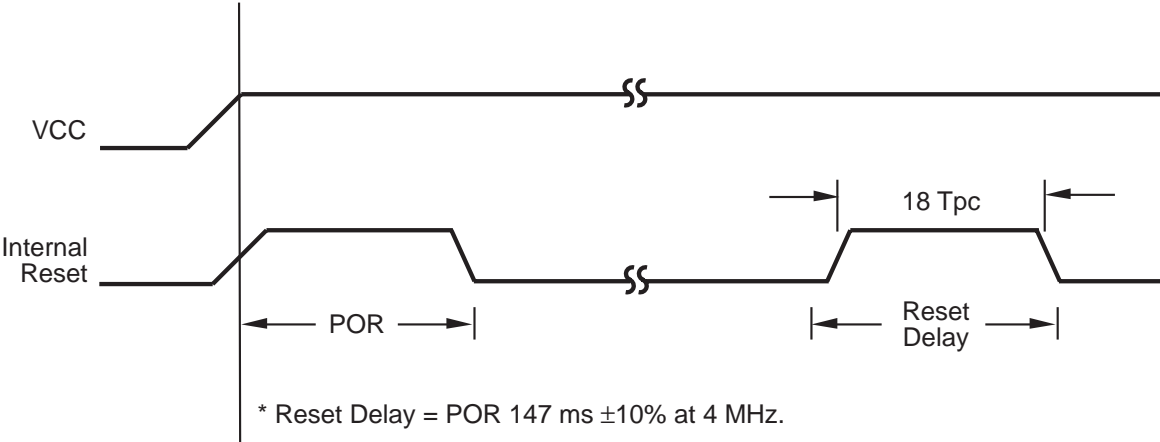


Figure 18. WDT Turn-On Timing After Reset

**PIN FUNCTIONS** (Continued)

**Power-On-Reset (POR).** A timer circuit is triggered by the system oscillator and is used for the Power-On Reset (POR) timer function. The POR time allows  $V_{CC}$  and the oscillator circuit to stabilize before instruction execution begins. POR period is defined as:

$$\text{POR (ms)} = \frac{589824}{f_{(\text{Hz})}}$$

The POR timer circuit is a one-shot timer triggered by one of two conditions:

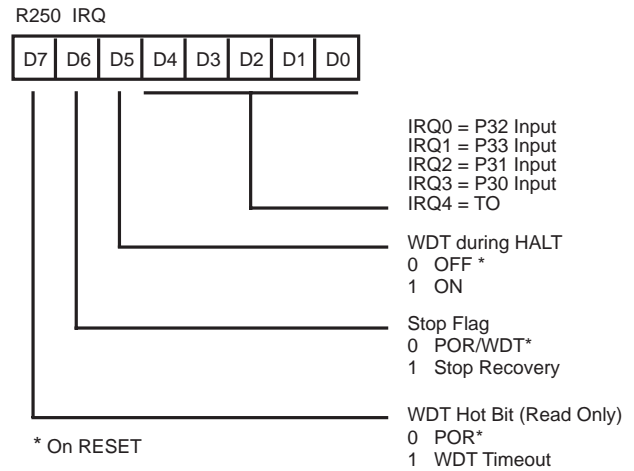
1. Power fail to Power OK status
2. Stop-Mode Recovery

The POR time is a nominal 147 ms  $\pm 10\%$ . At 4 MHz the POR timer is bypassed after Stop-Mode Recovery.

**HALT.** HALT turns off the internal CPU clock, but not the RC oscillator. The counter/timer and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The Z86K15 is recovered by interrupts, either externally or internally (Figure 19).

**STOP.** This instruction turns off the internal clock and oscillator. It reduces the standby current to less than 10  $\mu\text{A}$ . The STOP Mode is terminated by a reset only or external reset. This causes the processor to restart the application program at address 000C (HEX) or the active external interrupt vector. In order to enter STOP (or HALT) Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (Opcode=FFH) immediately before the appropriate sleep instruction, such as:

FF	NOP	; clear the pipeline
6F	STOP	; enter STOP Mode
		or
FF	NOP	; clear the pipeline
7F	HALT	; enter HALT Mode



**Figure 19. IRQ Register**

The Bit 6 of IRQ Registers are flags for STOP Mode Recovery (Figure 20).

**Cold or Warm Start (D6).** This bit is set upon entering STOP Mode. A 0 (cold) indicates that the device is awakened by a POR/WDT RESET. A 1 (warm) indicates that the device is awakened by a SMR source. This bit is reset when read.

Negative transition on any of the designated row input pins or host data line will recover Z86KXX from STOP Mode.



**Figure 20. Stop-Mode Recovery Source**

Z8® CONTROL REGISTER DIAGRAMS

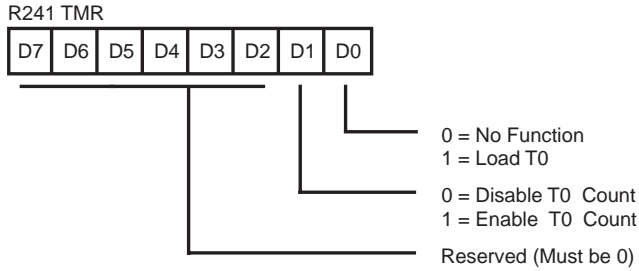
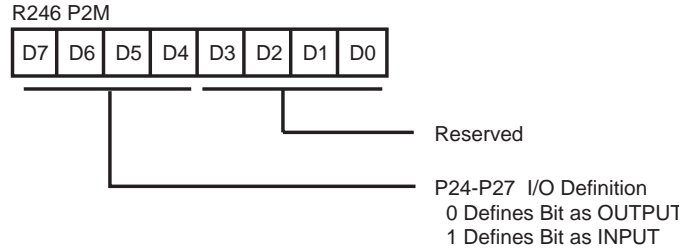
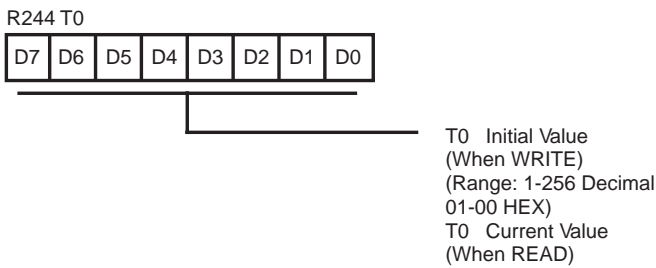


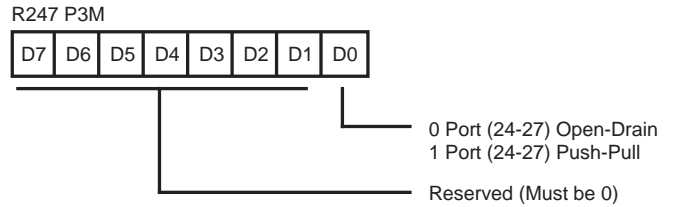
Figure 21. Timer Mode Register  
(F1<sub>H</sub>: Read/Write)



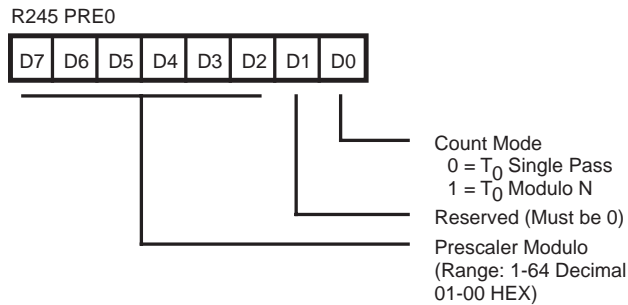
Port 2 Mode Register  
Figure 24. (F6<sub>H</sub>: Write Only)



Counter/Timer 0 Register  
Figure 22. (F4<sub>H</sub>: Read/Write)



Port 2 Open Drain Mode Register  
Figure 25. (F7<sub>H</sub>: Write Only)



Prescaler 0 Register  
Figure 23. (F5<sub>H</sub>: Write Only)

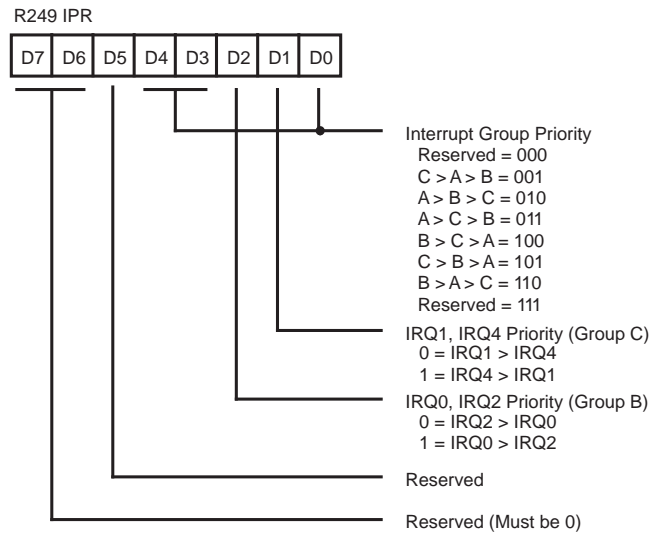
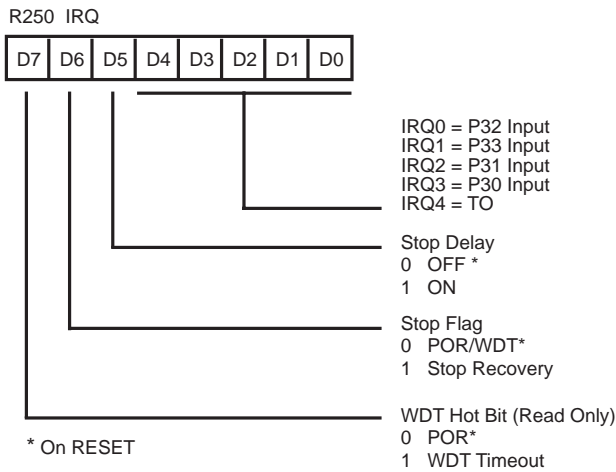
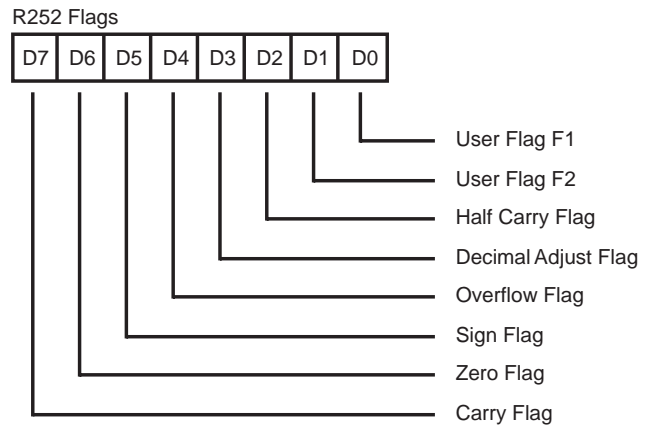


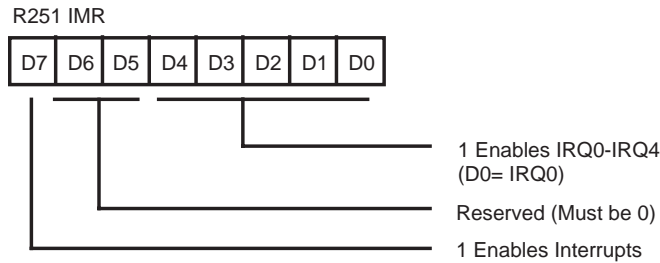
Figure 26. Interrupt Priority Register  
(F9<sub>H</sub>: Write Only)



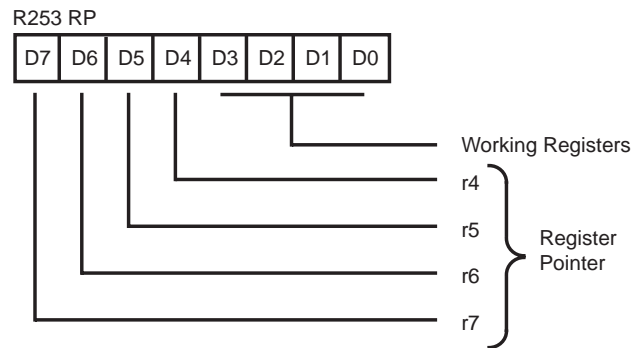
**Figure 27. Interrupt Request Register (FA<sub>H</sub>: Read/Write)**



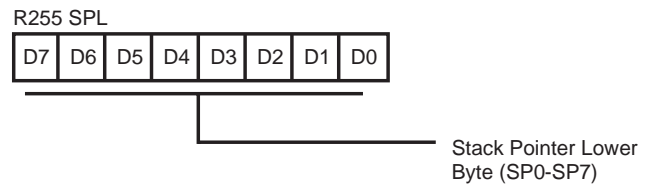
**Figure 29. Flag Register (FC<sub>H</sub>: Read/Write)**



**Figure 28. Interrupt Mask Register (FB<sub>H</sub>: Read/Write)**



**Register Pointer Figure 30. (FD<sub>H</sub>: Read/Write)**



**Stack Pointer Figure 31. (FF<sub>H</sub>: Read/Write)**

PACKAGE INFORMATION

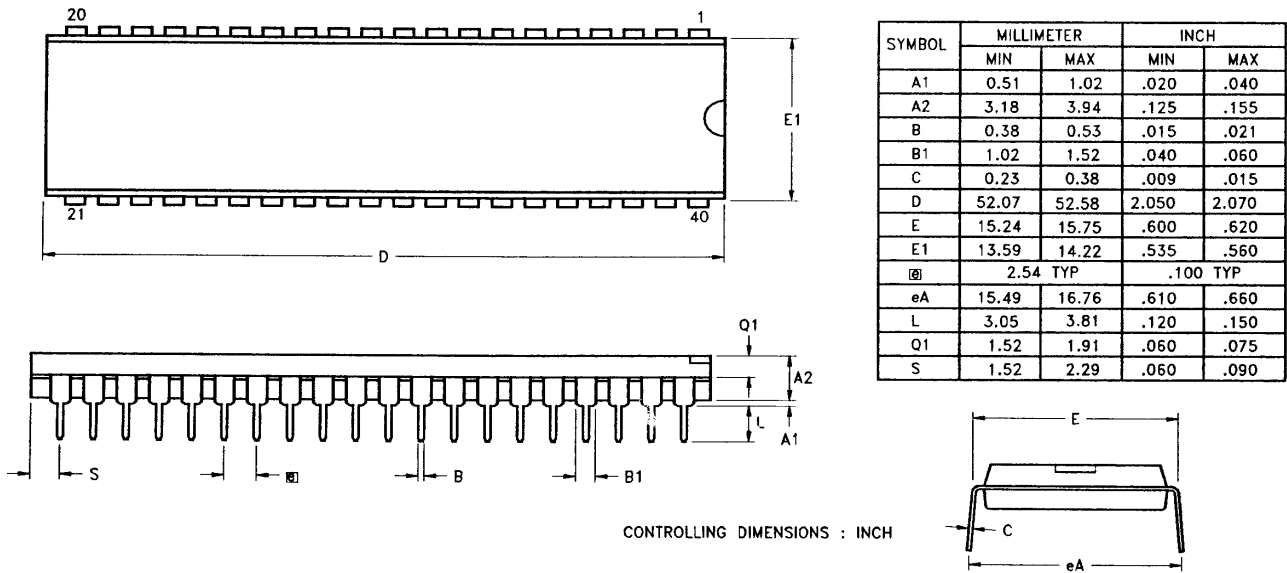


Figure 32. 40-Pin DIP Package Diagram

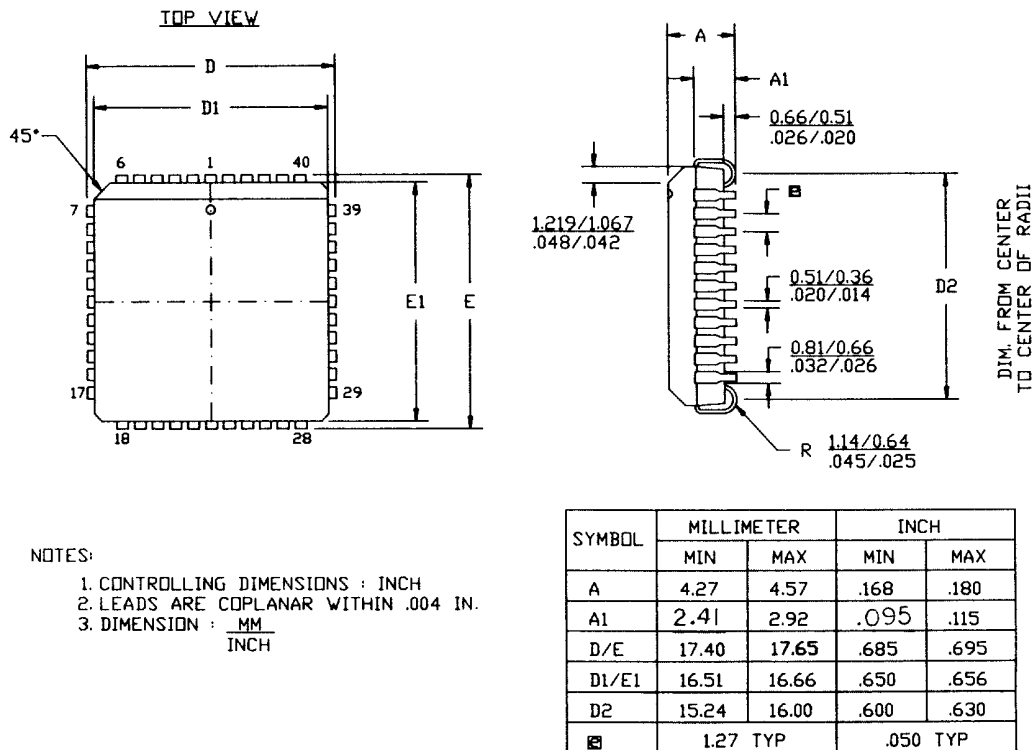
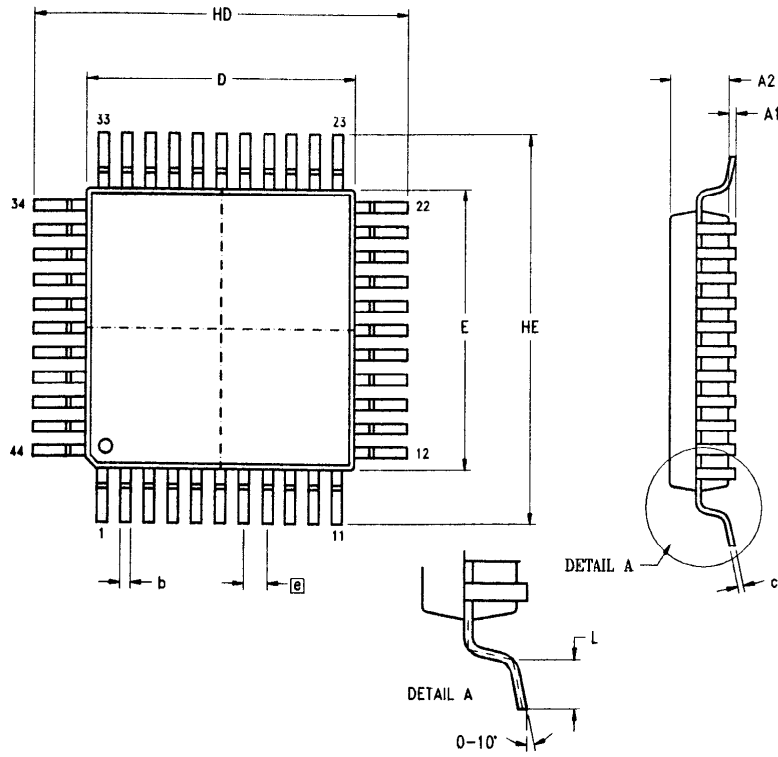


Figure 33. 44-Pin PLCC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
ⓐ	0.80 TYP		.0315 TYP	
L	0.60	1.20	.024	.047

NOTES:  
 1. CONTROLLING DIMENSIONS : MILLIMETER  
 2. LEAD COPLANARITY : MAX  $\frac{.10}{.004}$

Figure 34. 44-Pin QFP Package Diagram

**ORDERING INFORMATION**

**5 MHz**  
**40-Pin DIP**  
Z86KXX05PSC

**5 MHz**  
**44-Pin PLCC**  
Z86KXX05VSC

**5 MHz**  
**44-Pin QFP**  
Z86KXX05FSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

**CODES**

**Package**

P = Plastic DIP  
V = Plastic Leaded Chip Carrier  
F = Quad Flat Pack

**Speed**

05 = 5 MHz

**Environmental**

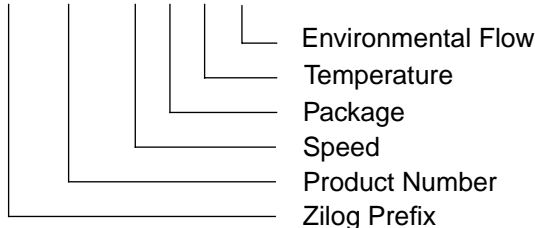
C = Plastic Standard

**Temperature**

S = 0°C to +70°C

**Example:**

Z 86K15 05 P S C is a Z86K15, 05 MHz, DIP, 0° to +70°C, Plastic Standard Flow



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