Dual 1 of 4 High Voltage Analog Switch

Ordering Information

V_{PP}-V_{NN}	Package Options	
	28-Lead Plastic Chip Carrier	Die
200V	HV20720PJ	HV20720X

Features

- ❑ HVCMOS® technology for high performance
- ❑ Operating voltage of up 200V
- ❑ Very low quiescent current-10µA
- ❑ Low parasitic capacitances
- ❑ Over 20MHz bandwidth
- ❑ -58dB typical output off isolation at 5MHz
- ❑ 5.0V CMOS logic circuitry
- ❑ Excellent noise immunity
- ❑ Flexible high voltage supplies

General Description

The Supertex HV207 is an 8-channel high-voltage analog switch integrated circuit (IC) configured as a dual 1 of 4 analog switch. The 2 sets of 4 analog switches are controlled independently with the 2 independent 1:4 decoders. The addressed switches are turned ON and the unaddressed switches are turned OFF. A logic high on the input clear pin will turn OFF all output switches regardless of the address input states.

Absolute Maximum Ratings*

V_{DD} Logic power supply voltage	-0.5V to +7.5V
V_{PP} - V_{NN} Supply voltage	+220V
V_{PP} Positive high voltage supply	-0.5V to +200V
V_{NN} Negative high voltage supply	+0.5V to -200V
Logic input voltages	-0.5V to V_{DD} +0.3V
V_{SIG} Analog Signal Range	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to +150°C
Power dissipation, 28 pin PLCC	1.2W

* All voltages are referenced to ground. Absolute maximum ratings are those values which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability.

11/12/01

Electrical Characteristics

DC Characteristics (V_{PP} = + 100V, V_{NN} = -100V, V_{DD} = + 5.0V, T_A = + 25°C)

Characteristics	Sym	min	typ	max	Units	Test Conditions
Small Signal Switch (ON) Resistance	R_{ONS}		22	27	Ω	V_{SIG} = 0V, I_{SW} = 5mA
Small Signal Switch (ON)Resistance Matching	ΔR_{ONS}		5.0	20	%	V_{SIG} = 0V, I_{SW} = 5mA
Voltage Drop Across SW at Large Positive V_{SIG}	ΔV_{SW}			15	V	V_{SIG} = +90V, R_L = 200Ω
Voltage Drop Across SW at Large Negative V_{SIG}	ΔV_{SW}			8.0	V	V_{SIG} = -90V, R_L = 200Ω
Switch Off Leakage Per Switch	I_{SOL}		1.0	10	µA	V_{SIG} = V_{pp} - 10V and V_{NN} + 10V
DC Offset Switch OFF			100	300	mV	R_L =100KΩ
DC Offset Switch ON			100	500	mV	R_L =100KΩ
Pos. HV Supply Current	I_{PPQ}		10	50	µA	All SWs OFF
Neg. HV Supply Current	I_{NNQ}		-10	-50	µA	All SWs OFF
Pos. HV Supply Current	I_{PPQ}		10	50	µA	All SWs ON, I_{SW} = 5 mA
Neg. HV Supply Current	I_{NNQ}		-10	-50	µA	All SWs ON, I_{SW} = 5 mA
Switch Output Peak Current			3.0	2.0	A	V_{SIG} duty cycle ≤0.1%
Output Switch Frequency	f_{SW}			50	Khz	Duty Cycle = 50%
I_{PP} Supply Current	I_{PP}		3.5	5.0	mA	4 SWs turning ON and OFF at 50KHz.
I_{NN} Supply Current	I_{NN}		-3.5	-5	mA	
Logic Supply Quiescent Current	I_{DDQ}			10	µA	

Electrical Characteristics

AC Characteristics (V_{PP} = + 100V, V_{NN} = - 100V, V_{DD} = + 5.0V, T_A = + 25°C)

Characteristics	Sym	min	typ	max	Units	Test Conditions
Turn On Time	t_{ON}			5.0	µs	V_{SIG} = V_{PP} - 10V, R_{LOAD} = 10KΩ
Turn Off Time	t_{OFF}			5.0	µs	V_{SIG} = V_{PP} - 10V, R_{LOAD} = 10KΩ
Maximum V_{SIG} Slew Rate	dv/dt			13	V/ns	
Off Isolation	KO	-45	-58		dB	f = 5.0MHz, R_{LOAD} = 50Ω
Switch Crosstalk	K_{CR}	-60			dB	f = 5.0MHz, R_{LOAD} = 50Ω
Output Switch Isolation Diode Current	I_{ID}			300	mA	300ns pulse width, 2.0% duty cycle

Operating Conditions

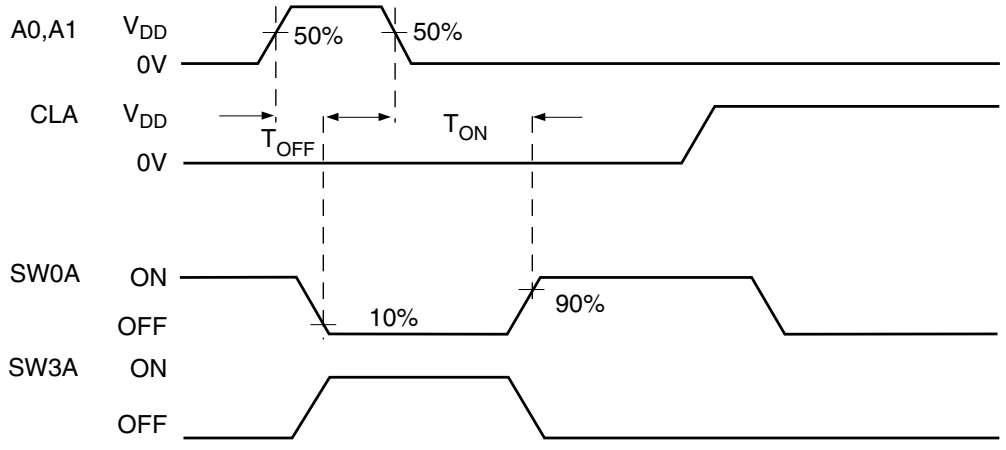
Symbol	Parameter	Value
V_{PP} - V_{NN}	Maximum differential voltage	+200V
V_{PP}	Positive high voltage supply[1]	+40V to V_{NN} + 200V
V_{NN}	Negative high voltage supply[1]	-40V to -160V
V_{DD}	Logic power supply voltage[1]	+4.75V to +5.25V
V_{IH}	High-level input voltage	V_{DD} -1.5V to V_{DD}
V_{IL}	Low-level input voltage	0V to 1.5V
V_{SIG}	Analog signal voltage peak-to-peak[2]	V_{NN} +10V to V_{PP} -10V
T_A	Operating free air-temperature	0°C to 70°C

Notes:
1 Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
2 V_{SIG} must be $V_{NN} \le V_{SIG} \le V_{PP}$ or floating during power up/down transistion.

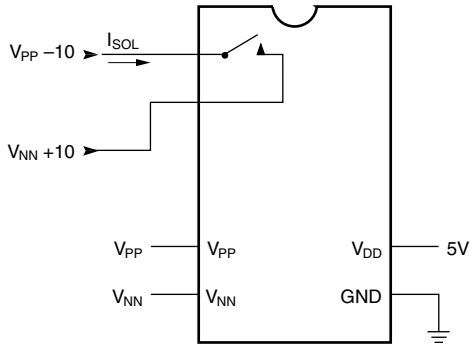
Truth Table

A1	A0	CLA	B1	B0	CLB	SW0A	SW1A	SW2A	SW3A	SW0B	SW1B	SW2B	SW3B
L	L	L	L	L	L	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF
L	H	L	L	H	L	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF
H	L	L	H	L	L	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF
H	H	L	H	H	L	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON
X	X	H	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

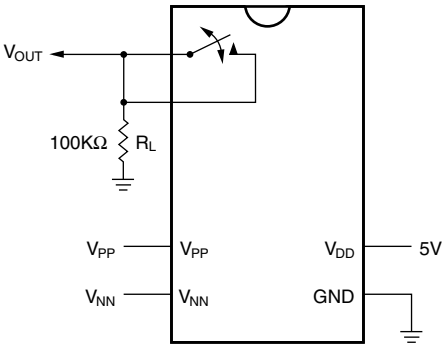
Logic Timing Waveforms



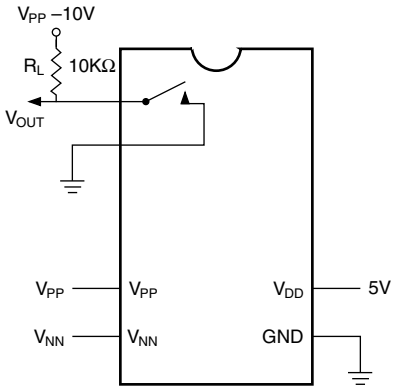
Test Circuits



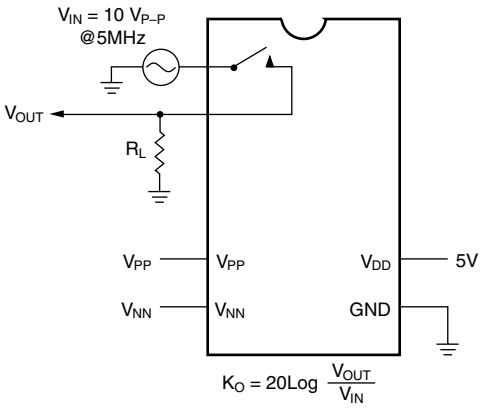
Switch OFF Leakage



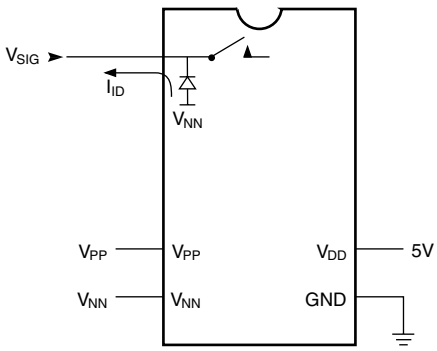
DC Offset ON/OFF



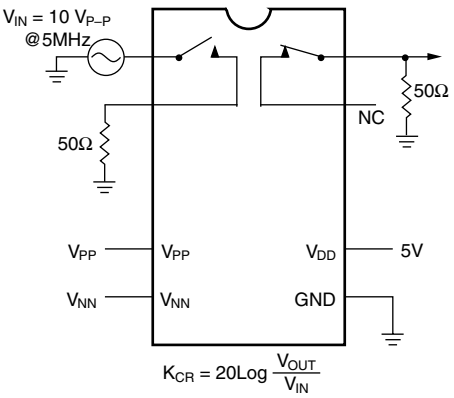
T_{ON}/T_{OFF} Test Circuit



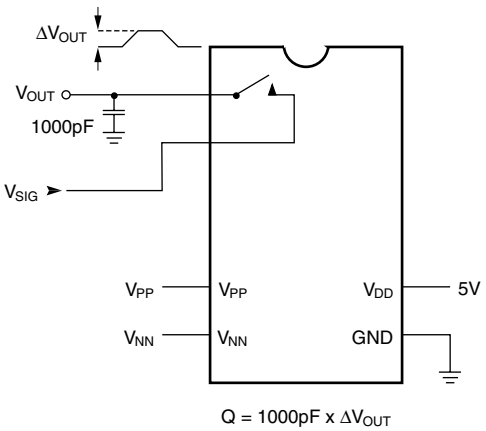
OFF Isolation



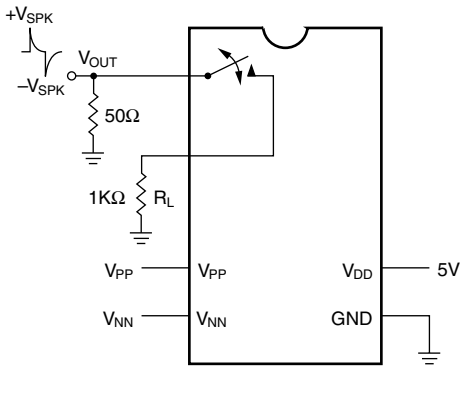
Isolation Diode Current



Crosstalk

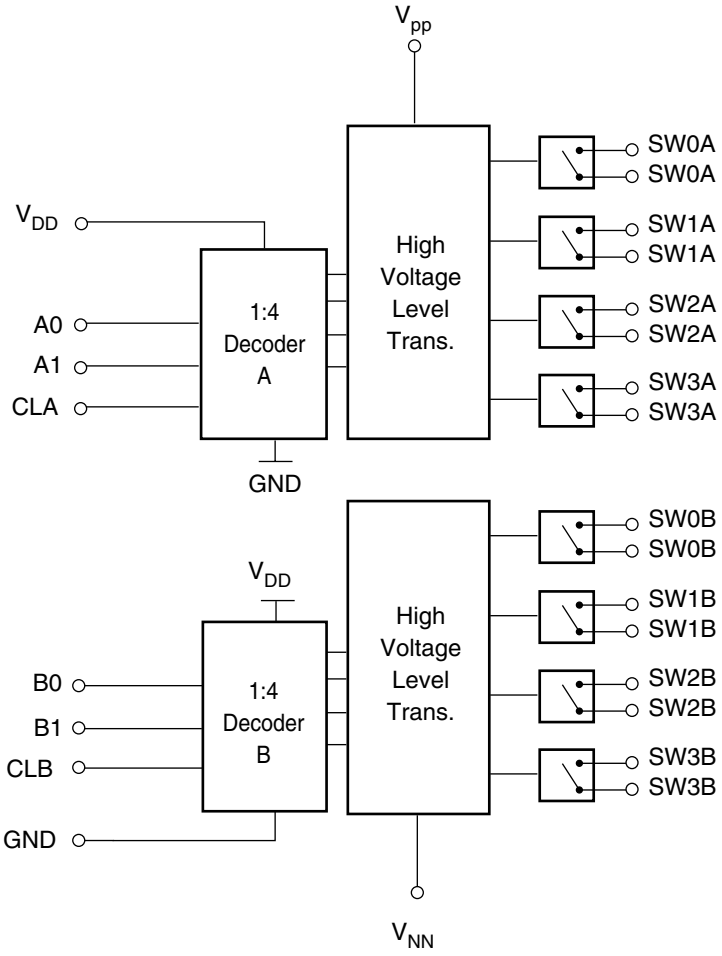


Charge Injection



Output Voltage Spike

Block Diagram

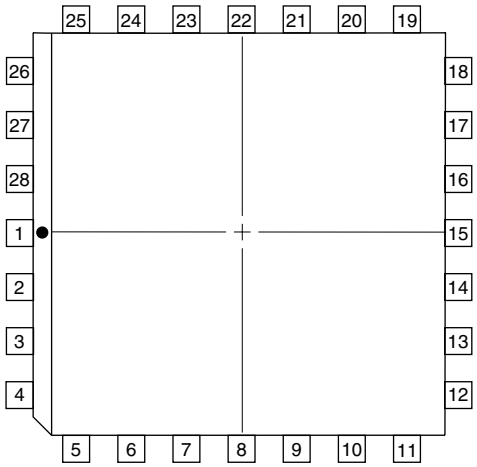


Pin Configuration

HV207 28-Pin J-Lead

Pin	Function	Pin	Function
1	SW3A	15	B1
2	SW2A	16	A0
3	SW2A	17	A1
4	SW1A	18	CLB
5	SW1A	19	CLA
6	SW0A	20	SW0B
7	SW0A	21	SW0B
8	N/C	22	SW1B
9	V_{PP}	23	SW1B
10	N/C	24	SW2B
11	V_{NN}	25	SW2B
12	GND	26	SW3B
13	V_{DD}	27	SW3B
14	B0	28	SW3A

Package Outline



top view

28-pin J-Lead Package

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