FAIRCHILD SEMICONDUCTOR™

July 1988
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100344
Low Power 8-Bit Latch with Cut-Off Drivers

General Description

The 100344 contains eight D-type latches, individual inputs (D_n), outputs (Q_n), a common enable pin ($\overline{E}$), latch enable ($\overline{LE}$), and output enable pin ($\overline{OEN}$). A Q output follows its D input when both $\overline{E}$ and $\overline{LE}$ are LOW. When either $\overline{E}$ or $\overline{LE}$ (or both) are HIGH, a latch stores the last valid data present on its D input prior to $\overline{E}$ or $\overline{LE}$ going HIGH.

A HIGH on $\overline{OEN}$ holds the outputs in a cut-off state. The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is −2.0V, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

The 100344 outputs are designed to drive a doubly terminated 50Ω transmission line (25Ω load impedance). All inputs have 50 kΩ pull-down resistors.

Features

- Cut-off drivers
- Drives 25Ω load
- Low power operation
- 2000V ESD protection
- Voltage compensated operating range = −4.2V to −5.7V

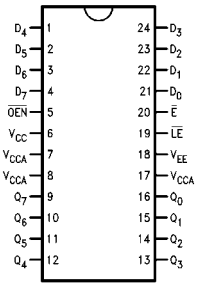
Ordering Code:

Order Number	Package Number	Package Description
100344PC	N24E	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
100344QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
100344QI	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Industrial Temperature Range (−40°C to +85°C)

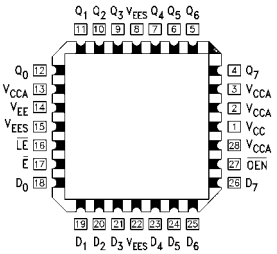
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

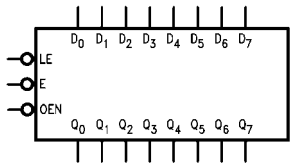
24-Pin DIP



28-Pin PLCC



Logic Symbol



Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{E}$	Enable Input
$\overline{LE}$	Latch Enable Input
$\overline{OEN}$	Output Enable Input
Q_0–Q_7	Data Outputs

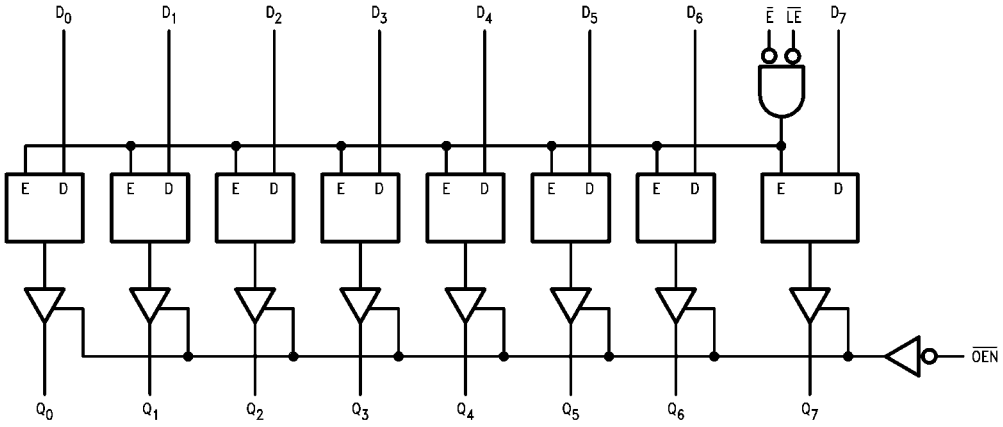
Truth Table

Inputs				Outputs
D_n	$\overline{E}$	$\overline{LE}$	$\overline{OEN}$	Q_n
L	L	L	L	L
H	L	L	L	H
X	H	X	L	Latched (Note 1)
X	X	H	L	Latched (Note 1)
X	X	X	H	Cutoff

H = HIGH Voltage level
L = LOW Voltage level
Cutoff = lower-than-LOW state
X = Don't Care

Note 1: Retains data present before either $\overline{LE}$ or $\overline{E}$ go HIGH.

Logic Diagram



Absolute Maximum Ratings (Note 2)

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−100 mA
ESD (Note 3)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°
Supply Voltage (V_{EE})	−5.7V to −4.2V

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: ESD testing conforms to MIL-STD-883, Method 3015.

Commercial Version

DC Electrical Characteristics (Note 4)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = V_{IH} (Max)	Loading with
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV	or V_{IL} (Min)	25Ω to −2.0V
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min)	Loading with
V_{OLC}	Output LOW Voltage			−1610	mV	or V_{IL} (Max)	25Ω to −2.0V
V_{OLZ}	Cutoff LOW Voltage			−1950	mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	$\overline{OEN}$ = HIGH
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			µA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current			240	µA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current					Inputs Open	
		−178		−85	mA	V_{EE} = −4.2V to −4.8V	
		−185		−85		V_{EE} = −4.2V to −5.7V	

Note 4: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output	0.90	2.10	0.90	2.10	1.00	2.30	ns	Figures 1, 2 (Note 5)
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$, $\overline{E}$ to Output	1.60	3.10	1.60	3.10	1.80	3.40	ns	Figures 1, 4 (Note 5)
t_{PZH}	Propagation Delay	1.60	4.20	1.60	4.20	1.60	4.20	ns	Figures 1, 2
t_{PHZ}	$\overline{OEN}$ to Output	1.00	2.70	1.00	2.70	1.00	2.70		(Note 5)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.00	0.45	2.00	0.45	2.00	ns	Figures 1, 3
t_S	Setup Time D_0–D_7	1.00		1.00		1.10		ns	Figures 1, 3
t_H	Hold Time D_0–D_7	0.10		0.10		0.10		ns	Figures 1, 3
t_{PW}(H)	Pulse Width HIGH $\overline{LE}$, $\overline{E}$	2.00		2.00		2.00		ns	Figures 1, 3

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Commercial Version (Continued)
PLCC AC Electrical Characteristics

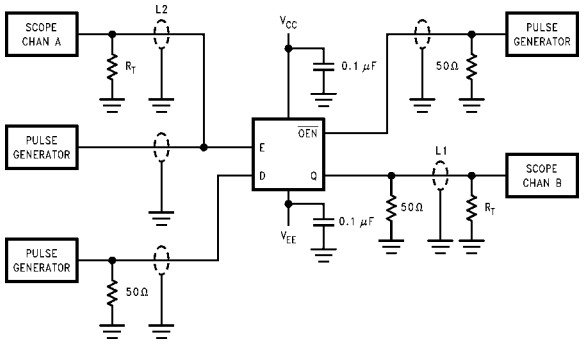
V_{EE} = –4.2V to –5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output	0.90	1.90	0.90	1.90	1.00	2.10	ns	Figures 1, 2 (Note 6)
t_{PLH} t_{PHL}	Propagation Delay $\overline{LE}$, $\overline{E}$ to Output	1.60	2.90	1.60	2.90	1.80	3.20	ns	Figures 1, 4 (Note 6)
t_{PZH} t_{PHZ}	Propagation Delay $\overline{OEN}$ to Output	1.60 1.00	4.00 2.50	1.60 1.00	4.00 2.50	1.60 1.00	4.00 2.50	ns	Figures 1, 2 (Note 6)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.90	0.45	1.90	0.45	1.90	ns	Figures 1, 3
t_S	Setup Time D_0–D_7	0.90		0.90		1.00		ns	Figures 1, 3
t_H	Hold Time D_0–D_7	0.00		0.00		0.00		ns	Figures 1, 3
t_{PW}(H)	Pulse Width HIGH $\overline{LE}$, $\overline{E}$	2.00		2.00		2.00		ns	Figures 1, 3
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		330		330		330	ps	PLCC Only (Note 7)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		330		330		330	ps	PLCC Only (Note 7)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		330		330		330	ps	PLCC Only (Note 7)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		230		230		230	ps	PLCC Only (Note 7)

Note 6: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Note 7: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}), or LOW-to-HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{ps} guaranteed by design.

Test Circuitry



Note:

- V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
- L1 and L2 = equal length 50Ω impedance lines
- R_T = 50Ω terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 25Ω to GND
- C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit

Switching Waveforms

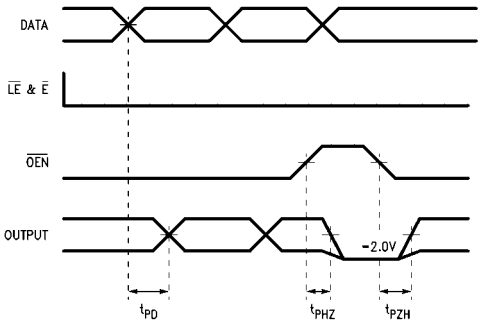


FIGURE 2. Propagation Delay and Cutoff Times

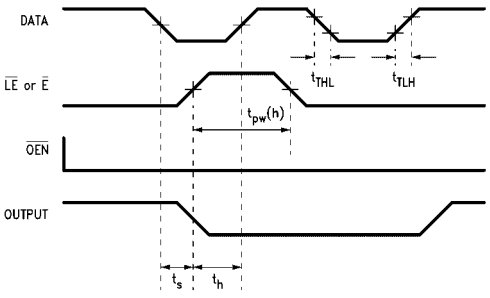


FIGURE 3. Setup, Hold and Pulse Width Times

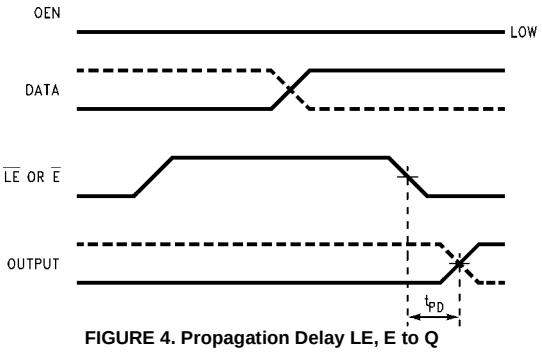
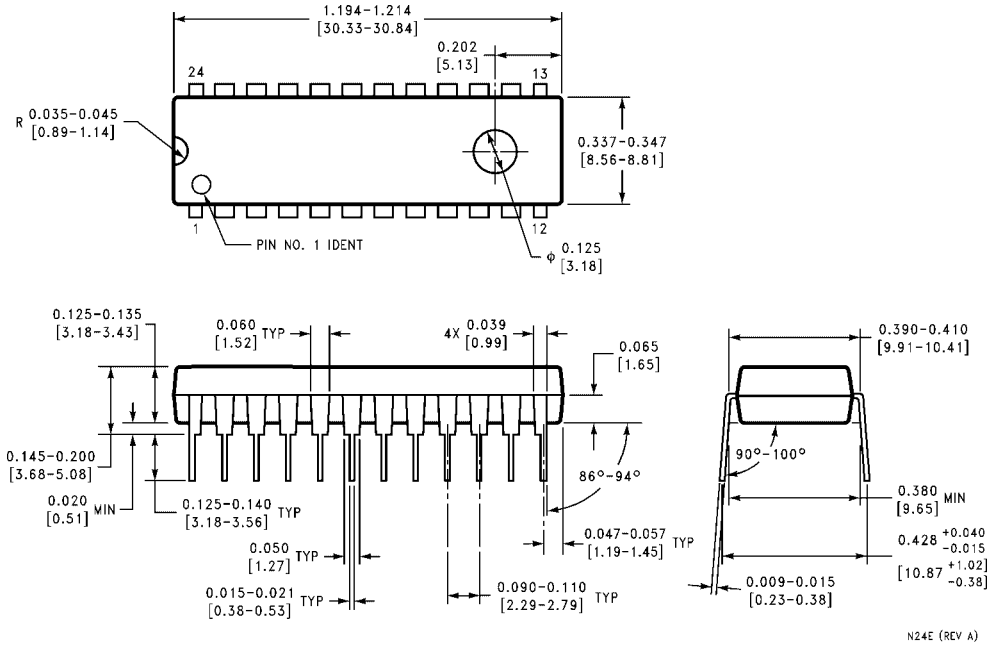


FIGURE 4. Propagation Delay LE, E to Q

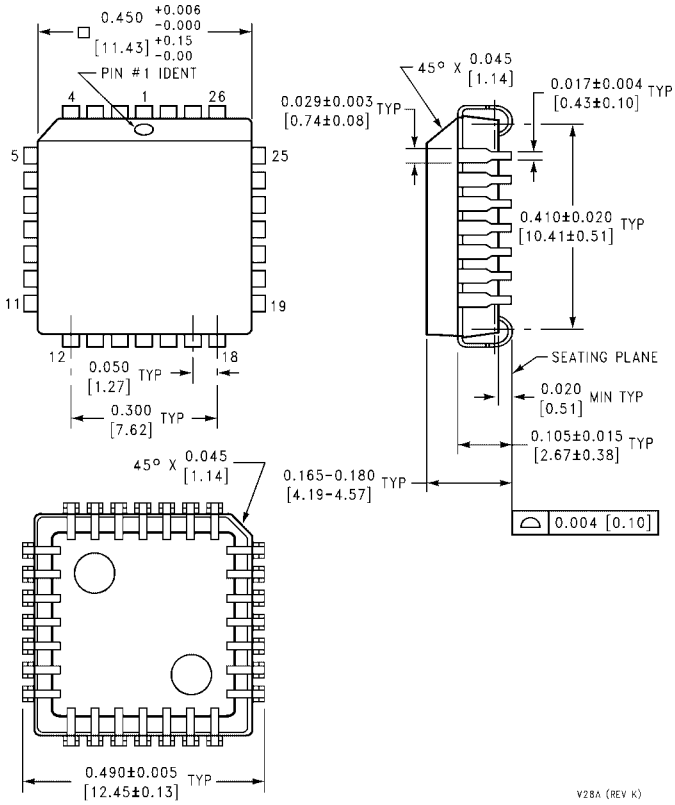
100344

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
Package Number N24E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
Package Number V28A