TH3122

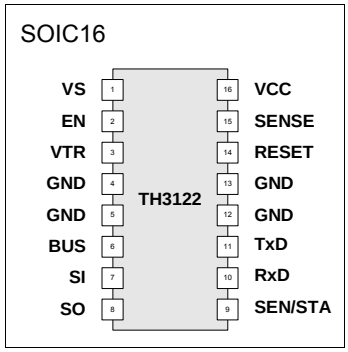
K-Bus Transceiver with integrated Voltage Regulator

Features and Benefits

- K-Bus Transceiver:
  - PNP-open emitter driver with slew rate control and current limitation
  - BUS input voltage -24V ... 30V (independently of V_S)
  - ISO 9141 and ODBII compliant
  - Possibility of BUS wake up
- Operating voltage V_S = 5.5 ... 16 V
- Very low standby current consumption <100 µA in normal mode (< 50 µA in sleep mode)
- Linear low drop voltage regulator:
  - Output voltage 5V± 2%
  - Output current max. 100mA
  - Output current limitation
- Overtemperature shutdown
- Configurable reset time (15ms/100ms) and reset threshold voltage (3.15V / 4.65V)
- Low voltage detection at VS
- Wake-up by K-BUS traffic and start-up capable independent of EN voltage level
- Universal comparator with an input voltage range –24V … 30V and digital output
- Load dump protected (40V)

Pin Diagram

SOIC16



Ordering Information

Part No.	***Temperature Range***	***Package***
TH3122	-40ºC...125ºC	SOIC16, 300mil

General Description

The TH3122 consists a low drop voltage regulator 5V/100mA and a K-Bus transceiver. The transceiver is suitable for K-Bus systems conform to ISO 9141.
The combination of voltage regulator and bus transceiver in combination with the monitoring functions make it possible to develop simple, but powerful and cheap nodes in K-Bus systems.
The wide output current area and the configurable reset time and reset voltage works together with many different microcontrollers.

Functional Diagram

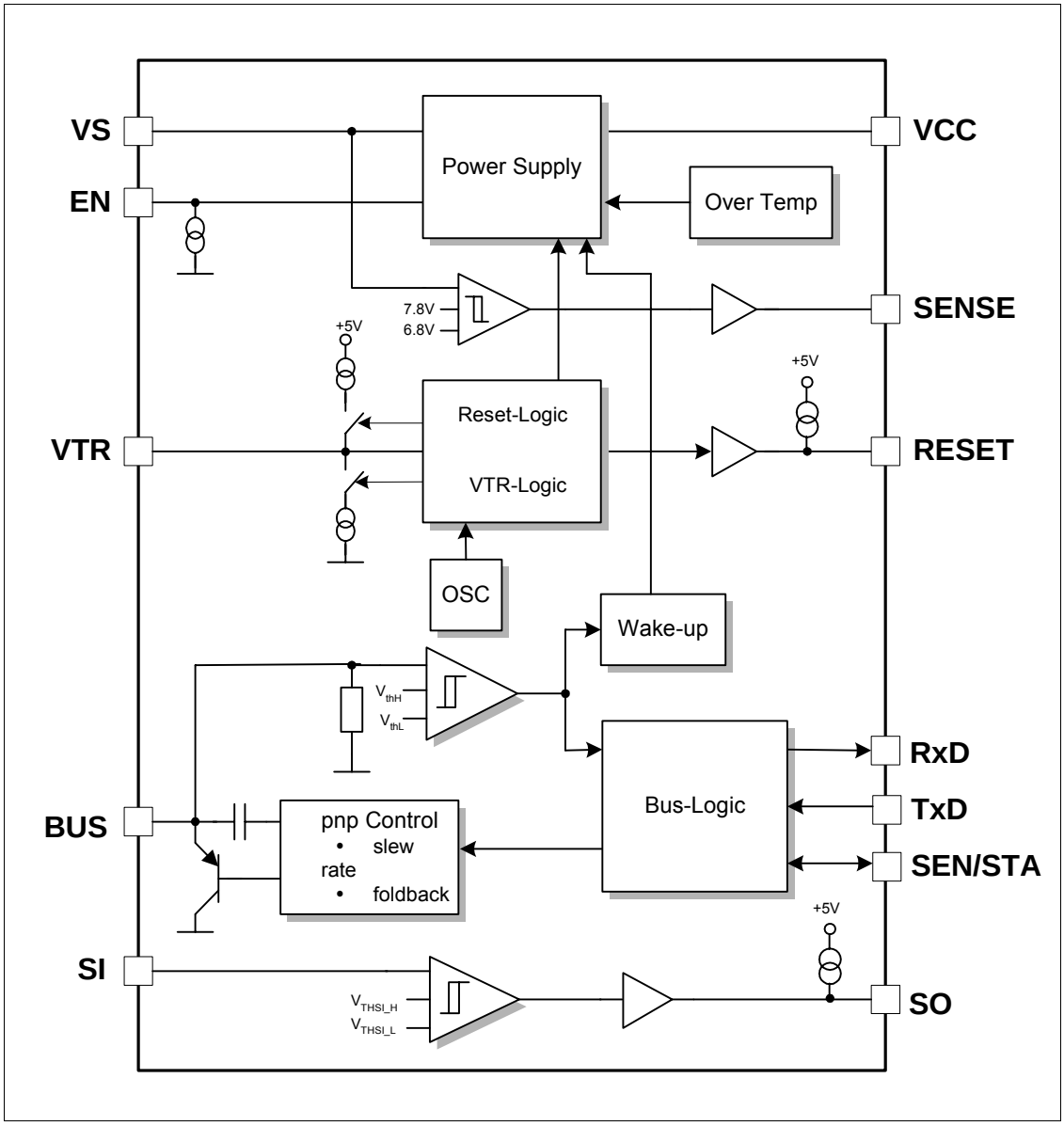


Figure 1 - Block Diagram

Functional Description

The TH3122 consists a voltage regulator 5V/100mA and a K-Bus transceiver, which is a bi-directional bus interface device for data transfer between K-Bus and the K-Bus protocol controller.

Also integrated into the transceiver are a voltage and time controlled reset management, power down, wake up function and a universal comparator for extended applications.

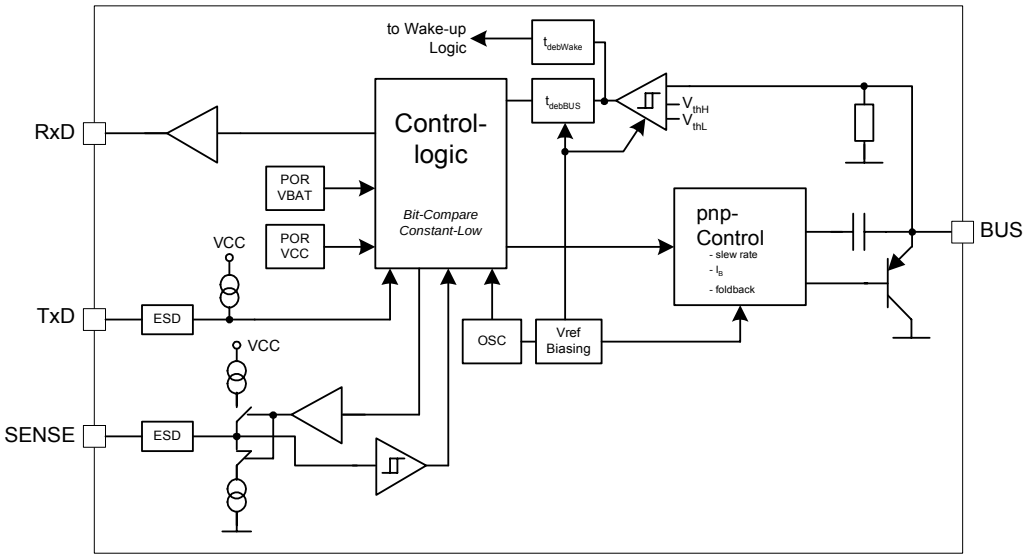


Figure 2 - Block Diagram K-Bus Transceiver

K-BUS Interface

The BUS Interface builds the connection between the serial 5V bus line of the protocol controller and the 12V K-Bus line.
The transceiver consists a pnp-driver with slew rate control and fold-back characteristic and consists as well in the receiver a high voltage comparator followed by a debouncing unit.

Transmit Mode

During the transmission the data at the pin TxD will be transferred to the pin BUS. To minimize the electromagnetic emission of the bus line, the TH3122 has an integrated slew rate control.

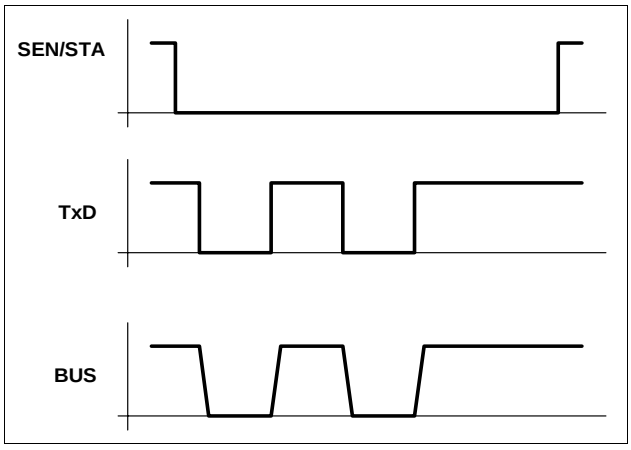


Figure 3 - Transmit Mode Pulse Diagram

Receive Mode

The data at the pin BUS will be transferred to the pin RxD. Short spikes on the bus signal are suppressed by the implemented debouncing circuit.

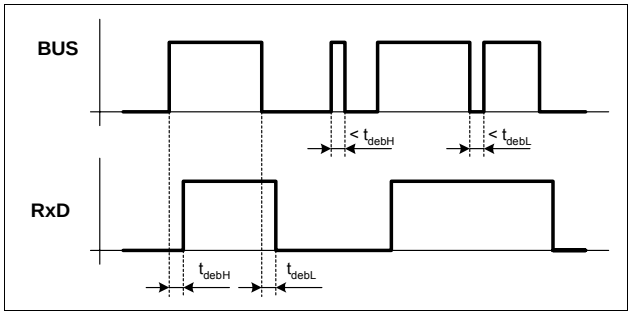


Figure 4 - Receive Mode Pulse Diagram

Bit Compare

Are the signals at the pin TxD and the pin BUS within a specified time t_{bc} not identical, the transmission will be interrupted.
If both signals at TxD and BUS are “High” within the time t_{ena} the transmission will be enabled. The bit-compare-function is activ when the pin SEN/STA is open (not overwritten).

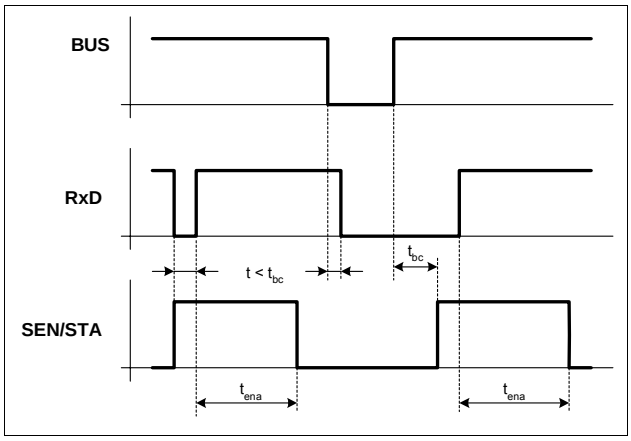


Figure 5 - Bit Compare Pulse Diagram

SEN/STA

The pin SEN/STA is bidirectional. Used as an output the pin indicates whether the transmit-path is enabled or disabled:

SEN/STA =”0”
transmission path is enabled
SEN/STA =”1”
transmission path is disabled

Using this pin as an input the transmission path can be overwritten (independent of bit-compare and constant-low function):

SEN/STA=”0”
forcing the transmission path free
SEN/STA=”1”
disable the transmission path

Constant Low Switch Off

A falling edge at pin TxD (from “1” to “0”) starts the internal constant low timer (SEN/STA open).
If the low level “0” is valid for the time t_{low} the transmission unit of the TH3122 will be disabled.
The receive unit is still active. A high level “1” at TxD with a minimum pulse width of t_{rec} reset the constant low timer.
Transmitting is possible not until TxD and BUS is High for the time t_{ena}.

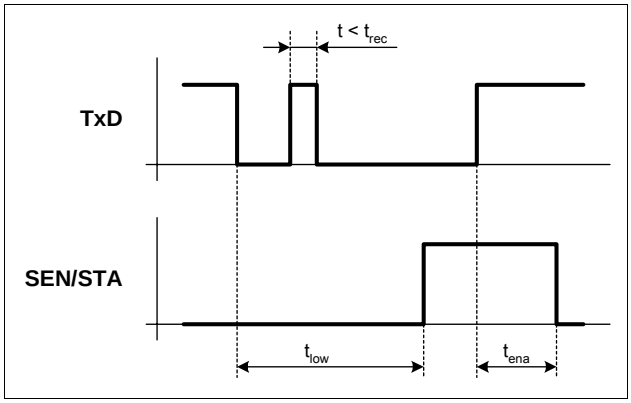


Figure 6 - Constant Low Pulse Diagram

Linear Regulator and Controlling Functions

Regulator

The TH3122 has an integrated linear regulator with an output voltage of 5V ±2% and an output current of max. 100mA. The regulator is switched on or off with a signal on the EN pin or wake up with a BUS signal.

Initialization

The initialization is started if the power supply is switched on, or after the temperature limitation has switched off the regulator or in case of BUS traffic (wake up).

If the V_{CC} voltage level is higher than V_{RESEIN}, the reset time t_{RES} is started. This reset time is determined by the voltage level on the VTR pin (see table VTR Programming). After t_{RES} a rising edge on the RESET output is generated (see figure 7 - Initialization).

The regulator is active and can only switched off with a falling edge on EN. The regulator remain with EN=high in active mode and therefore also the V_{CC} voltage is active.

The input EN has an internal pull down resistor. If EN=high, the internal pull down current is switched off to minimize the quiescent current.

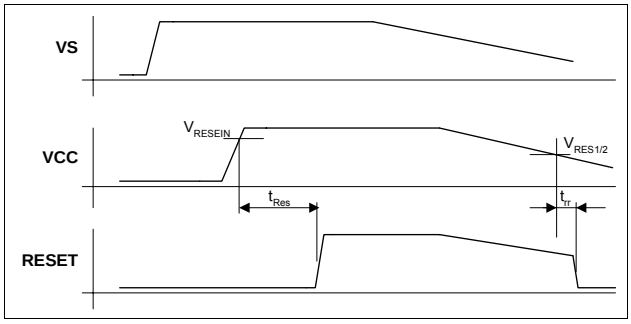


Figure 7 - Initialization

RESET Output

The RESET output is switched from low to high if V_S is switched on and V_{CC}>V_{RESEIN} after the time t_{RES}.

If the voltage V_{CC} drop below V_{RES1} or V_{RES2} then the RESET output is switched from high to low after the time t_{rr} has been reached.

The voltage level for V_{RES1} and V_{RES2} and the corresponding times t_{RES} can be programmed via the analogue input VTR.

Wake up with BUS traffic

If the regulator is put in standby mode it can be wake up with the BUS interface. Every pulse on the BUS (high pulse or low pulse) with a pulse width of min. 45µs will switch on the regulator.

After the BUS has wake up the regulator, it can only be switched off with a high level followed by a low level on the EN pin.

Reset Programming on VTR

With the VTR pin the reset switch off levels and delay time can be programmed.

The voltage on VCC influences the reset function.

VTR-Programming

The voltage on VTR input is read out if the voltage at this pin is higher than V_{RESEIN} . This value defines the reset switch off voltage V_{RES}. With the next oscillator cycle it switch on the pull up current source if VTR=low or the pull down current source if VTR=high. The sources are active for one oscillator cycle. The level changes during this procedures on VTR, which depends on the external pull up or pull down resistors control the reset time t_{Res}

VTR-Mode	V_{RES}	t_{Res}
VTR = GND	V_{RES} = V_{RES1} = 3.15V	100ms
VTR = VCC	V_{RES} = V_{RES2} = 4.65V	100ms
VTR with R ≥ 50kΩ to GND	V_{RES} = V_{RES1} = 3.15V	15ms
VTR with R ≥ 50kΩ to VCC	V_{RES} = V_{RES2} = 4.65V	15ms

Temperature Limitation

If the junction temperature 150ºC < T_j < 170ºC the over temperture recognition will be active and the regulator voltage and the BUS driver will be switched off. After T_j fall below 140ºC the TH3122 will be initialized, independently of the voltage levels on EN and BUS.

The function of the TH3122 is possible between T_{Amax} and the switch off temperature, but small parameter differences can appear.

Low Voltage Detection V_S

Low voltage on V_S is monitored on SENSE output.

If V_S has reached the level of V_S =6.8V then the SENSE output generates low level. The normal operating range is V_S > 7.8V and the SENSE output generates a high level.

Universal Comparator

The TH3122 consist a universal comparator for general use. The positive input of this comparator is connected to the pin SI. The input voltage range of SI is 0V...V_S. The input voltage is compared with a fixed reference voltage at high or low level and the comparator output SO drives a 5V digital signal.

Application Hints

Operating during Disturbances

The absence of V_S ,V_{CC} or GND connection or ground shift either alone or in any combination, do not influence or disturb the communication between other bus nodes.

Undervoltage

The reset unit secures the correct behavior of the driver during undervoltage. The inputs have pull-up or pull-down characteristics and have therefore defined voltage levels.

With $4.5V \leq V_{CC} \leq 5.25V$ the bus connection operates within the correct parameters .

If $V_{RES1} \leq V_{CC} \leq 4.5V$ the TxD signal is transmitted to the bus. The receive mode is also activ.

If $V_{CC} < V_{RES1}$the bus driver is tristate.

SENSE and SO output the correct signal if $V_{CC} > V_{RES}$. The specificated values of the input voltages on SO can't guaranteed.

Regulator Circuitry

The choice and dimension of the capacitor on VCC is determined by application point of view. Important parameters are the current difference on load changes and the maximum short time voltage drop.

The VCC pin must be connected to a min. 2µF capacitor for stable operating of the regulator in the whole operating range.

Short Circuit Proof

All in- and outputs are short circuit proof to battery and ground. A thermal shut down circuit prevent VCC and BUS from any damage.

Baud Rate

The TH3122 has a maximum Baud rate of 9600 Baud ($C_{BUS} < 25nF$, $R_{PU} > 400\Omega$).

Application Circuitry

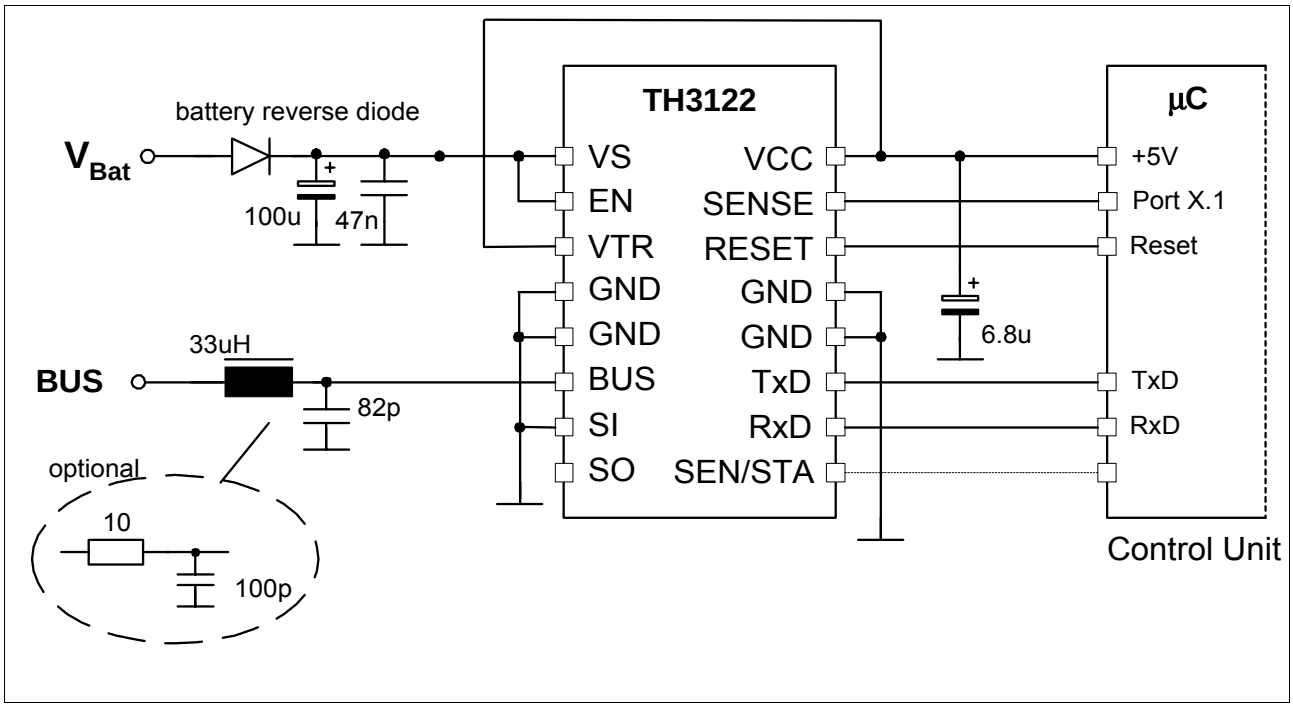


Figure 8 - Application Circuit

There should be used an LC-Filter to minimize the influence of EMI on the BUS lines.

Electrical Specification

All voltages are referenced to ground (GND). Positive currents flow into the IC. The absolute maximum ratings given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may affect the reliability of the device. Reliable operation of the TH3122 is only specified within the limits shown in ”Operating conditions”.

Operating Conditions

Parameter	Symbol	Min	Max	Unit
Battery voltage	V_S	5.25	16	V
Supply voltage	V_{CC}	4.75	5.25	V
Operating ambient temperature	T_A	-40	+125	°C
Junction temperature [1]	T_J		+150	°C

Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage at VS [2]	V_S		-1.0	16	V
		T ≤ 1min	-	30	
		T ≤ 500 ms	-	40	
Input voltage at pin BUS [2]	V_{INBUS}		-24	30	V
		T ≤ 500 ms	-	40	
Difference VS-VCC	V_{S-VCC}		-0.3	40	V
Input voltage at pin EN and SI	V_{INENSI}		-0.3	V_S+0.3	V
Input voltage at pin VTR, TxD, SEN/STA, SO, RESET, SENSE	V_{IN}		-0.3	V_{CC}+0.3	V
Input current at pin EN, VTR, SI, SO, SEN/STA, TxD, RxD, RESET, SENSE	I_{IN}		-25	25	mA
Input current for short circuit of pin VS and VCC	I_{Short}		-500	500	mA
Power dissipation T_A = 85 °C [3]	P_0			600	mW
Thermal resistance from junction to ambient	R_{THJA}			50	K/W
Junction temperature [4]	T_J			150	°C
Storage temperature	T_{STG}		-55	150	°C

[1] Junction temperature is defined in IEC 747-1
[2] The current and voltage values are valid independent from each other.
[3] The maximum power dissipation is defined by the ambient temperature and the thermal resistance. It can be calculated with $P_0 = (V_S - V_{CC}) * I_{VCC} + P_{BUS}$. P_{BUS} is the BUS driver output with normally ≤25 mW
[4] see over temperature protection

Static Characteristics

(V_S = 5.25 to 16V, V_{CC}= 4.75 to 5.25V, T_A = -40 to +125°C, unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Linear Regulator						
Output voltage VCC	V_{CCn}	5.5V ≤ V_S ≤ 16V T_A = 25°C	4.95	5.0	5.05	V
	V_{CCt}	5.5V ≤ V_S ≤ 16V	4.90	5.0	5.10	V
	V_{CCh}	V_{SUP} > 16V	4.95	5.0	5.25	V
	V_{CCl}	3.3 V< V_S< 5.5 V	V_S-V_D		5.1	V
Supply current, „normal mode“	I_{Snl}	V_{EN} = V_S = 12V, Pins 8-11, 14-16 open			100	µA
Supply current, „sleep mode“	I_{Ssleep}	V_{EN} = 0V, V_{CC} switched off		35	50	µA
Drop-out voltage	V_D	V_S ≥ 4.0V, I_{VCC} = 25mA			200	mV
		V_S ≥ 4.0V, I_{VCC} = 100mA			400	mV
		V_S ≥ 3.3V, I_{VCC} = 20mA			600	mV
Output current VCC	I_{VCC}	V_S ≥ 3.0V	100			mA
Current limitation VCC	I_{LVCC}	V_S > 0V			300	mA
Load capacity	C_{load}	ESR ≤ 5Ω	2			µF
Power-on-reset threshold “V_{CC} on”	V_{RESEIN}	refered to V_{CC}, V_S > 4.6V	4.5	4.65	4.8	V
Power-on-reset threshold “V_{CC} off”	V_{RES2}	VTR=High, V_S > 0V	4.5	4.65	4.8	V
	V_{RES1}	VTR=Low, V_S > 0V	3.0	3.15	3.3	
SENSE-Output						
VS - threshold low at SENSE	V_{SENL}		6.8			V
VS - threshold high an SENSE	V_{SENH}				7.8	V
Hysteresis SENSE	V_{SENHYS}		100			mV
Output voltage low	V_{OL}	I_{OUT} = 1mA			0.8	V
Output voltage high	V_{OH}	I_{OUT} = -1mA	V_{CC}-0.8			V
Enable-Input EN						
Input voltage low	V_{ENL}		-0.3		1.75	V
Input voltage high	V_{ENH}		2.5		V_S +0.3	V
Hysteresis	V_{ENHYS}		100			mV
Pull-down current EN	I_{pdEN}	V_{EN} > V_{ENH}	1.8	4.0	7.5	µA
		V_{EN} < V_{ENL}	70	100	130	µA
Output RESET						
Output voltage low	V_{OL}	I_{OUT} = 1 mA, V_{SUP} > 5.5 V			0.8	V
		10 kΩ RESET to VCC V_S = V_{CC} = 0.8 V			0.2	V
Pull-up current	I_{pu}		-500	-375	-250	µA

Static Characteristics (continued)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Comparator SI, SO						
Threshold low SI	V_{IL}		1.05	1.16		V
Threshold High SI	V_{IH}			1.21	1.4	V
Hysteresis	V_{HYS}		30			mV
Output voltage low at SO	V_{OL}	I_{OUT} = 1 mA, V_S > 5.5 V			0.8	V
		10 kΩ SO to VCC, V_{CC} > 3.3V			0.4	V
Pull-up current at SO	I_{pu}		-500	-375	-250	µA
Input VTR						
Threshold low	V_{TRL}		0.15	0.25		V_{CC}
Threshold high	V_{TRH}			0.75	0.85	V_{CC}
Output current low	I_{OL}	V_{CC} > 3.3 V	160	230	300	µA
Output current high	I_{OH}		-300	-230	-160	µA
K-Bus-Interface						
Power-on-reset threshold	V_{POR}	V_{POR} =V_{RES1}	3.0	3.15	3.3	V
Pull-up current TxD	I_{pu}		-500	-375	-250	µA
Pull-down current SEN/STA	I_{pdSEN}		250	375	500	µA
Pull-up current SEN/STA	I_{puSEN}		-500	-375	-250	µA
Input voltage low TxD, SEN/STA	V_{IL}				0.25	V_{CC}
Input voltage high TxD, SEN/STA	V_{IH}		0.75			V_{CC}
Input voltage low BUS	V_{IL}				0.45	V_S
Input voltage high BUS	V_{IH}		0.55			V_S
Hysteresis BUS	V_{HYS}			50		mV
Input restistance BUS	R_{INBUS}	0 ≤ V_{BUS} ≤ 40 V	400	600	1500	kΩ
		0 ≤ V_{BUS} ≤ 40 V T_A ≤125 °C			1300	
		V_{BUS} = -25V T_A ≤125 °C	60			
Output voltage BUS	V_{BUS}	V_S = 12V, SENSE = low			1.2	V
		V_S = 12V, SENSE = low			1.0	
Current limitation BUS	I_{LIM}	V_{BUS} > 2.5V	40		100	mA
Output voltage low RxD	V_{OL}	I_{OUT} = 1 mA			0.8	V
Output voltage high RxD	V_{OH}	I_{OUT} = -1mA	V_{CC}-0.8			V

Dynamic Characteristics

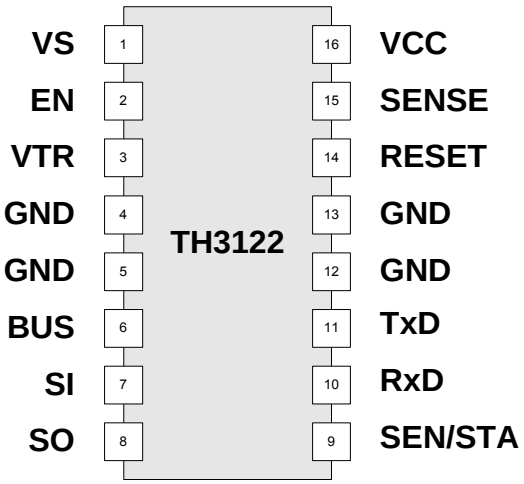
All dynamic values of the table below refer to the test-schematic schown in Figure 3 - Test Circuit for Dynamic Characteristics

For the definition of delay and transitions times see Figure 2 - TH8060 Timing Diagram.

($5.25V \le V_S \le 16V$, $4.75V \le V_{CC} \le 5.25V$, $-40°C \le T_A \le 125°C$, unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
RESET						
Reset time	t_{Res}	R_{VTR} < 1 kΩ	70	100	140	ms
		R_{VTR} > 45 kΩ	10	15	20	ms
Reset rising time	t_{rr}		3.0	6.5	10	µs
K-Bus-Interface						
Slew rate BUS falling edge	dV/dT_{fall}		-2.2	-1.6	-1.0	V/µs
Slew rate BUS rising edge	dV/d_{Trise}		1.0	1.6	2.2	
Symmetry of Slew rate BUS	dV/dT_{sym}				0.3	V/µs
Debouncing time BUS	t_{debBUS}	High pulse or low pulse	1.5	2.8	4.0	µs
Symmetry of debouncing BUS	t_{debsym}				0.5	µs
Propagation delay TxD -> RxD	t_{pd}				20	µs
Symmetry of propagation delay TxD -> RxD	t_{pdsym}				3.5	µs
Bit compare time BUS, SENSE, TxD	t_{bc}		35	52	70	µs
Recovery time BUS, TxD	t_{rec}		30	50	75	µs
Inhibit time for transmit BUS, TxD	t_{ena}		0.92	1.33	1.8	ms
Constant low switch off BUS, TxD	t_{low}		3	6	12	ms
Oscillator frequency	f_{OSC}		8	12	15	kHz
Debouncing time TxD	t_{deb}		0.6	1.0	1.5	µs
Debouncing time EN	t_{deb}		200			ns
Wake-up debouncing BUS	$t_{debWake}$		25	45	90	µs
Propagation delay SI -> SO	t_{pdcomp}		4		11	µs
Debouncing VS-SENSE	t_{deb}		10	17	25	µs

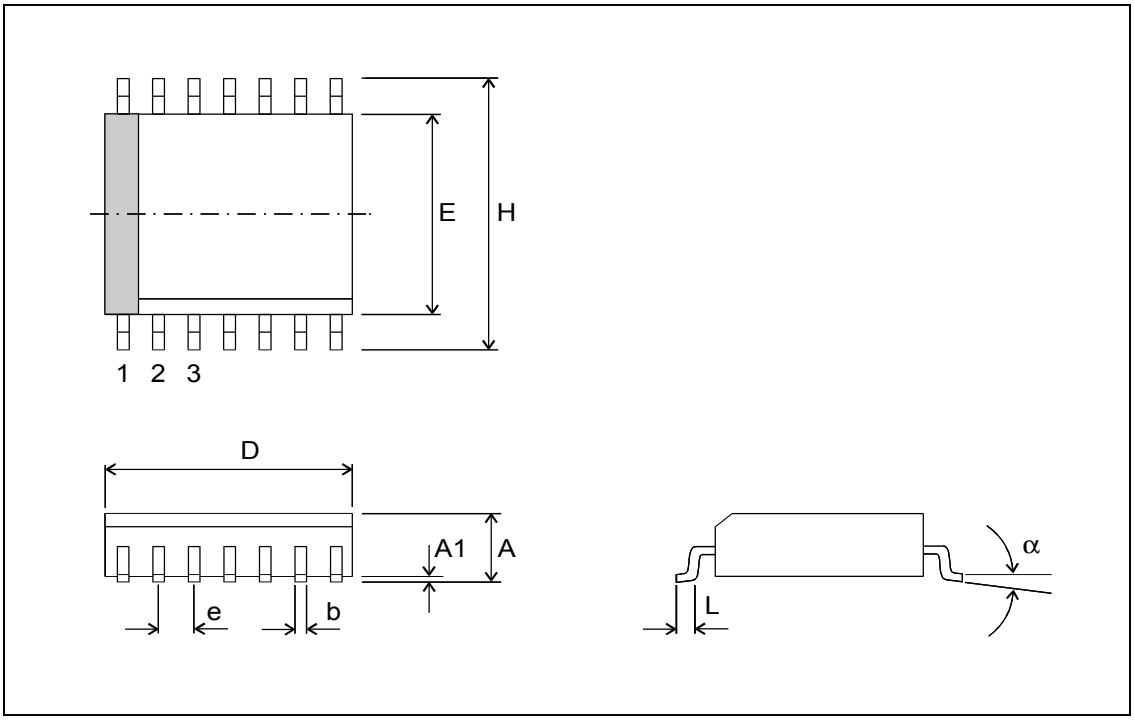
Pin Description



Pin	Name	I/O	Function
1	VS		Supply voltage
2	EN	I	Enable Input voltage regulator, HV-pull-down-Input, High-active
3	VTR	I	Analogue Input - definition of reset time und Reset voltage level
4	GND		Ground
5	GND		Ground
6	BUS	I/O	Bi-directional bus line
7	SI	I	Comparator Input, HV-Input
8	SO	O	5V-Comparator Output
9	SEN/STA	I/O	Send status
10	RxD	O	Receive Output, 5V-push-pull
11	TxD	I	5V-Transmit Input, pull-up-Input
12	GND		Ground
13	GND		Ground
14	RESET	O	5V-output reset, active low
15	SENSE	O	5V-output of VS-Monitoring
16	VCC	O	Regulator output 5V/100mA

Mechanical Specifications

SOIC16 Package Dimensions



Small Outline Integrated Circiut (SOIC), SOIC 16, 300 mil

All Dimension in mm, coplanarity < 0.1 mm									
	D	**E**	**H**	**A**	**A1**	**e**	**b**	**L**	**α**
min	10.1	7.40	10.00	2.35	0.10	1.27	0.33	0.40	0°
max	10.5	7.60	10.65	2.65	0.30		0.51	1.27	8°
All Dimension in inch, coplanarity < 0.004”									
min	0.398	0.291	0.394	0.093	0.004	0.050	0.013	0.016	0°
max	0.413	0.299	0.419	0.104	0.012		0.020	0.050	8°

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